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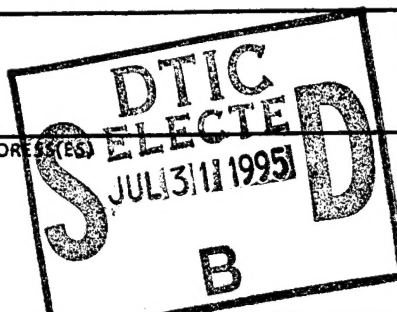
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13. ABSTRACT (Maximum 200 words)

We have successfully fabricated and tested two types of high temperature superconducting Josephson junctions on silicon. An assessment of the properties of these junctions shows that they are attractive candidates for rf applications. Step-edge SNS junctions fabricated with gold barriers exhibited the ac Josephson effect to over 100 GHz, with the power and frequency dependence of the current voltage characteristics in good quantitative agreement with the resistively shunted junction model. The resistances of these junctions were of order 1 ohm, and critical currents over 0.1 mA were obtained. Critical currents were observed to 76 K. Electron-beam modified Josephson weak links were also demonstrated on silicon. These devices exhibited microwave induced steps in the current voltage characteristics, magnetic interference patterns with strong central maxima, and sinusoidal magnetic interference patterns when imbedded in dc SQUIDS.

We have also identified an approach to relieve thermal expansion stress in HTS films on silicon that would allow the fabrication of filters and other passive components with greatly improved performance at significantly lower cost than current techniques.

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2. INTRODUCTION

2.a. Identification and Significance of the Problem or Opportunity

Modern rf systems are increasingly pushing the performance limits of conventional electronic materials. Because of their high speed and low loss, dissipation and dispersion, superconducting thin films and devices present unique opportunities for new applications in telecommunications, signal processing, radiometric sensing and high speed instrumentation[1]. In this arena, passive HTS components have demonstrated superior performance compared to thin film copper, gold or aluminum devices from dc to mm wave frequencies[2]. These new devices have been shown to significantly improve system performance and reduce size, weight and power dissipation relative to conventional components. On the other hand, more sophisticated system level rf components such as receiver front-ends, correlators, convolvers, spectrum analyzers and downconverters have been retarded by the lack of monolithically compatible active devices. This situation is changing as recent advances in HTS Josephson junction technology [3-11] have introduced new possibilities for high speed active HTS devices. To fully exploit these developments, however, advances in manufacturability, reproducibility, and substrate materials are necessary.

In many potential HTS applications, one would prefer to use HTS devices for critical high speed functions such as receiver front-ends, mixers, filters and delay lines, but use "conventional" silicon and III-V semiconductors for complex logic, active devices and other analog components. At present, this can only be done in difficult to manufacture hybrid packages, in part because suitable Josephson devices have not been successfully fabricated on silicon substrates, the industry workhorse for microelectronics. Metal oxides such as the perovskites lanthanum aluminate (LaAlO_3) and strontium titanate (SrTiO_3) have so far been the most successful substrate materials from the viewpoint of Josephson junction fabrication [4-12], but these are incompatible with monolithically packaged silicon circuits. In addition, the loss, dispersion, limited size, high dielectric constants and high costs of the oxide substrates are problematic for rf applications, particularly for high operating frequencies and wafer scale integrated components.

In a broad sense, full realization of the potential of advanced HTS electronics will be achieved with a manufacturable **monolithic** technology capable of integrating high speed silicon electronics (i.e. cooled CMOS), with active and passive HTS devices such as Josephson mixers, oscillators, logic, IR detectors[13], SQUIDs, delay lines, resonators, filters, and interconnects. The most direct route to this goal is to develop an HTS Josephson technology compatible with industry standard silicon substrates. To achieve this, continued improvements in the quality and availability of HTS thin films and devices on silicon are necessary.

Although the benefits to be obtained through an effective integration of HTS and silicon components could be pervasive and far reaching, there are, however, two main hurdles to overcome before silicon can be adopted as a general purpose substrate for HTS electronics:

- The lack of a good Josephson technology on silicon restricts the full integration of HTS with conventional electronics.
- HTS film thicknesses on silicon substrates are currently limited to approximately 75 nm or less due to stress induced cracking caused by the thermal expansion mismatch between the films and substrates. These limitations impact the the manufacturability of multilayered structures (e.g. crossovers and transmission lines), as well as the rf properties (e.g. the kinetic inductance and surface resistance) of the films themselves.

2.b. The Innovation

Monolithic HTS Josephson Junction Technology on Silicon Substrates

The principle objective of this program was to solve the problem of Josephson junction availability on silicon. During the program, we also identified an innovative approach to solving the film stress problem that could allow the fabrication of multilayered HTS structures with much thicker films.

The junction process developed in Phase I is suitable for monolithic integration of Josephson electronics with passive HTS and conventional silicon transistor technology. The many resulting benefits afforded by the adoption of silicon are summarized below:

- Lower cost (especially for wafer scale rf subsystems)
- Better dielectric properties than metal oxide substrates (resulting in higher Q resonators, sharper filters, lower insertion loss, reduced power requirements)
- Transparent from infrared to microwave frequencies (at cryogenic temperatures)
- Integrable with VLSI silicon, high-speed III-V, and HTS components
- Exploits an extensive preexisting silicon technology base

In Phase I we demonstrated fabrication of two types of Josephson junctions depicted in Fig. 1 on silicon substrates: **Step edge SNS junctions** and **Electron Beam Modified Microbridges**. The two approaches are distinguished from each other primarily by the properties of the barrier separating the superconducting electrodes. In the step edge SNS junctions, the barrier is formed from a noble metal bridge deposited across a gap in a superconducting film grown over a step[3-5]. The barrier for an electron beam modified (EBM) junction is formed from modified HTS material itself, by rastering a narrow high energy (~120 KeV) electron beam over a lithographically produced microconstriction in an HTS film[7, 9]. Details on fabrication will be described in section 3. In previous work, both types of junctions showed promise for rf and other high speed applications: Work by the P.I. and coworkers at NIST demonstrated the ac Josephson effects in step-edge SNS junctions on LaAlO_3 substrates to frequencies up to 8 THz [3], and at Stony Brook, Gurvitch et al have demonstrated a working rapid single flux quantum (RSFQ) rs flip-flop from e-beam modified junctions on lanthanum aluminate substrates[12].

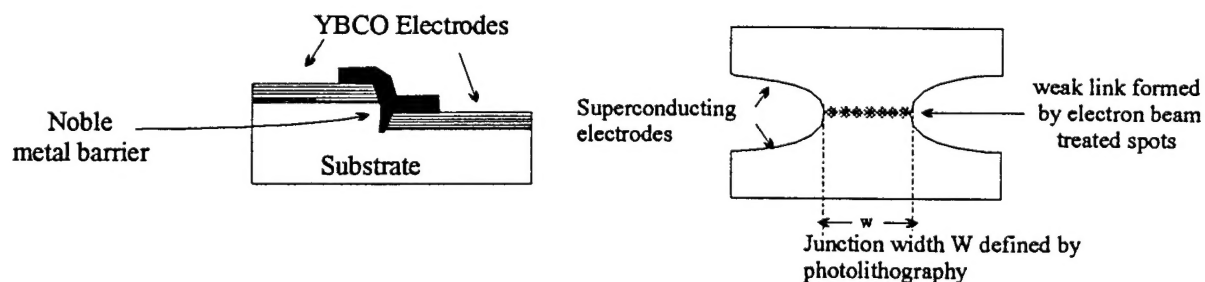


Fig. 1 (a) Cross section of step edge SNS junction on silicon. **(b)** Top view of electron beam modified Josephson junction on silicon.

Film Stress

As mentioned above, the problem of film stress is particularly severe for HTS films grown on yttria stabilized zirconia (YSZ) buffered silicon substrates. As a general rule, the YSZ buffered HTS films deposited directly on silicon are under tensile strain after cooldown, and crack when the total HTS thickness exceeds approximately 75 nm. Many laboratories find it difficult to grow even 35 nm thick films of YBCO on silicon without cracking. Because the stress limited maximum film thickness is smaller than the superconducting London penetration depth, the parasitic kinetic inductance and surface resistance of HTS structures on silicon are increased. This will degrade the performance of filters, resonators, transmission lines and other passive components, and there is thus a strong motivation to improve the technology for HTS films on silicon by increasing the allowable thicknesses to 200 nm or greater. A solution to the film stress problem identified during Phase I is based on developing a novel compliant substrate fabricated by wafer bonding. This would be developed in a Phase II program as described in section 4. **If successful in this as well as in junction fabrication, we will have eliminated the two most significant barriers opposing widespread adoption of silicon substrates for HTS electronics.**

2.c. Phase I Technical Objectives

The overall objectives of Phase I were to establish: 1) the potential for HTS Josephson junctions on silicon wafers, 2) a demonstration of a Josephson component integrated monolithically on a silicon wafer, 3) Appropriate circuit models for Josephson junctions on silicon, and 4) a preliminary study of more sophisticated Josephson based components to identify appropriate Phase II target devices. These program objectives will be met by accomplishing four tasks, with partial objectives as follows:

Task 1 - Josephson Junction Fabrication - Fabricate Josephson junctions on silicon substrates with properties tailored for microwave applications.

Task 2 - Josephson Junction Characterization - Measure electrical properties of Josephson junctions at dc and microwave frequencies. Measure temperature dependence of critical current and resistance.

Task 3 - Device Modeling - Develop circuit models for microwave Josephson devices on silicon coupled to passive HTS components.

Task 4 - Demonstration Circuits - Demonstrate a monolithic HTS circuit on silicon coupling active Josephson elements with a (passive) transmission line resonator. Initiate design study for an integrated microwave downconverter.

2.d. Summary of Phase I Accomplishments

Step-Edge SNS Josephson Junctions on silicon substrates:

- A rotatable substrate heater assembly was constructed and utilized for SNS junction depositions at AFR.
- Working in collaboration with the group at NIST, **we successfully fabricated the world's first step-edge SNS Josephson junctions on step-edges fabricated in silicon substrates.** Scanning electron micrographs of a Josephson chip on silicon are shown in Fig. 2.

- Critical current vs temperature curves of the step-edge junctions were measured and critical currents were observed to 76 K.
- Microwave induced Shapiro steps in the current-voltage characteristics were observed to 100 GHz.
- The rf power dependence of the critical current and Shapiro steps was measured.
- The rf power dependence of the current-voltage characteristic was found to be in quantitative agreement with the resistively shunted junction model.

Electron Beam modified Josephson junctions on silicon substrates:

- Working in collaboration with Professor Michael Gurvitch at the State University **we have successfully fabricated the worlds first electron beam modified Josephson junction from YBCO films deposited on silicon substrates.**
- Critical current vs temperature curves of the e-beam modified junctions were measured and critical currents were observed to 79 K.
- DC Superconducting Quantum Interference Devices (SQUIDs) were fabricated from e-beam modified junctions on silicon substrates, and sinusoidal voltage modulation was observed.
- Penetration depths of the HTS films were estimated from the SQUID modulation depth.

Film Stress and related technology:

- High quality yttria stabilized zirconia (YSZ) buffered YBCO films with thicknesses to 75 nm were grown on both reactively ion etched and pristine silicon surfaces after native oxide removal and passivation by spin etching. Up to these thicknesses, the films showed no cracks due to thermal expansion coefficient mismatch.
- A novel compliant substrate based on silicon-on-insulator (SOI) technology has been identified that would allow the growth of low stress HTS thin films and multilayers on silicon substrates. The new substrate technology might eliminate film stress as a problem for films thicker than 75 nm.

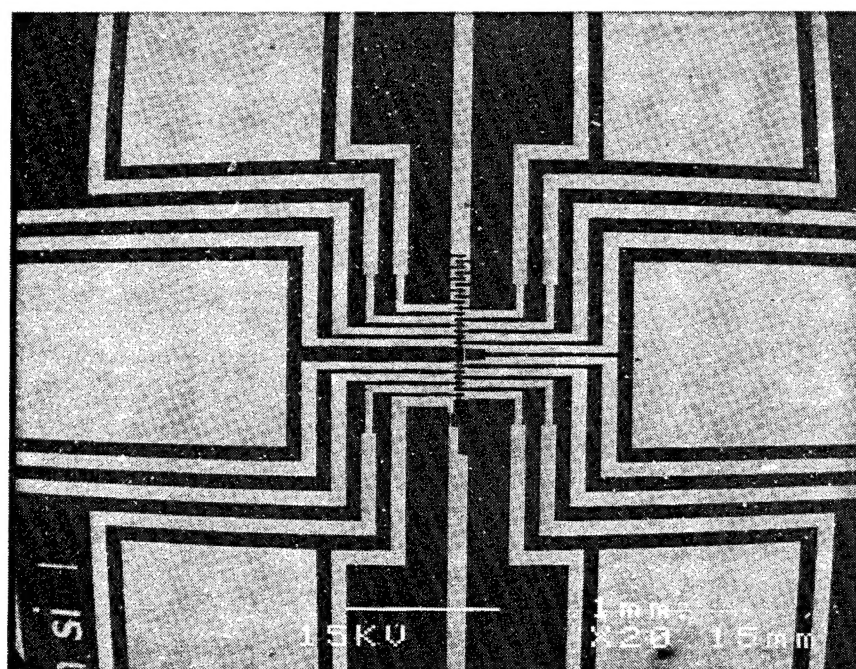
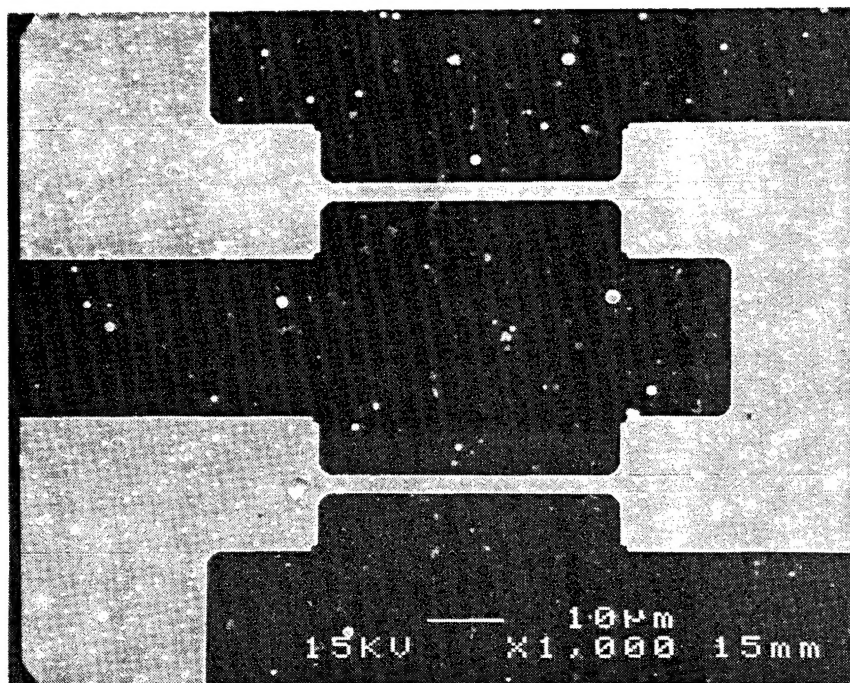


Fig. 2. SEM images of an HTS step-edge SNS chip with 14 junctions and a junction array, fabricated on a silicon substrate. The lower image is a plan view of the chip, the upper image is a magnified view of two of the junctions.

2.e. Technical Background

1) HTS thin films on silicon:

A process for growing high quality epitaxial HTS films on buffer layers on silicon has been developed [13-16] and is utilized routinely at Advanced Fuel Research for its work in bolometric infrared detectors. A facility for growth of HTS films by pulsed laser deposition (PLD) on Si wafers was established at AFR, Inc. in early 1991. The AFR deposition system is illustrated schematically in Fig. 3. Silicon wafers and Si compounds react chemically with $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ (YBCO) at film growth temperatures [15], so a buffer layer of yttria-stabilized zirconia (YSZ) is first grown epitaxially on the Si wafer surface. Preparation of the fresh Si surface must also be included in the process, since all Si surfaces are coated with a native oxide that spoils epitaxy unless it is removed [16]. We have shown that YSZ buffered HTS films grown by PLD at AFR are of high crystallographic and electronic quality as evidenced by their narrow omega rocking curves (0.6 degrees), and their high critical currents ($J_c \sim 3 \times 10^6 \text{ A/cm}^2$). A cross section transmission electron micrograph of a YSZ buffered YSZ film on a silicon substrate is shown in Fig. 4. In addition to the sharp interfaces, note that there is a thin amorphous SiO_2 layer evident under the YSZ film even though the native oxide was stripped with HF just before deposition. Interestingly enough, this layer forms after the YSZ layer has nucleated and does not disrupt the epitaxy of either the YSZ or HTS thin films.

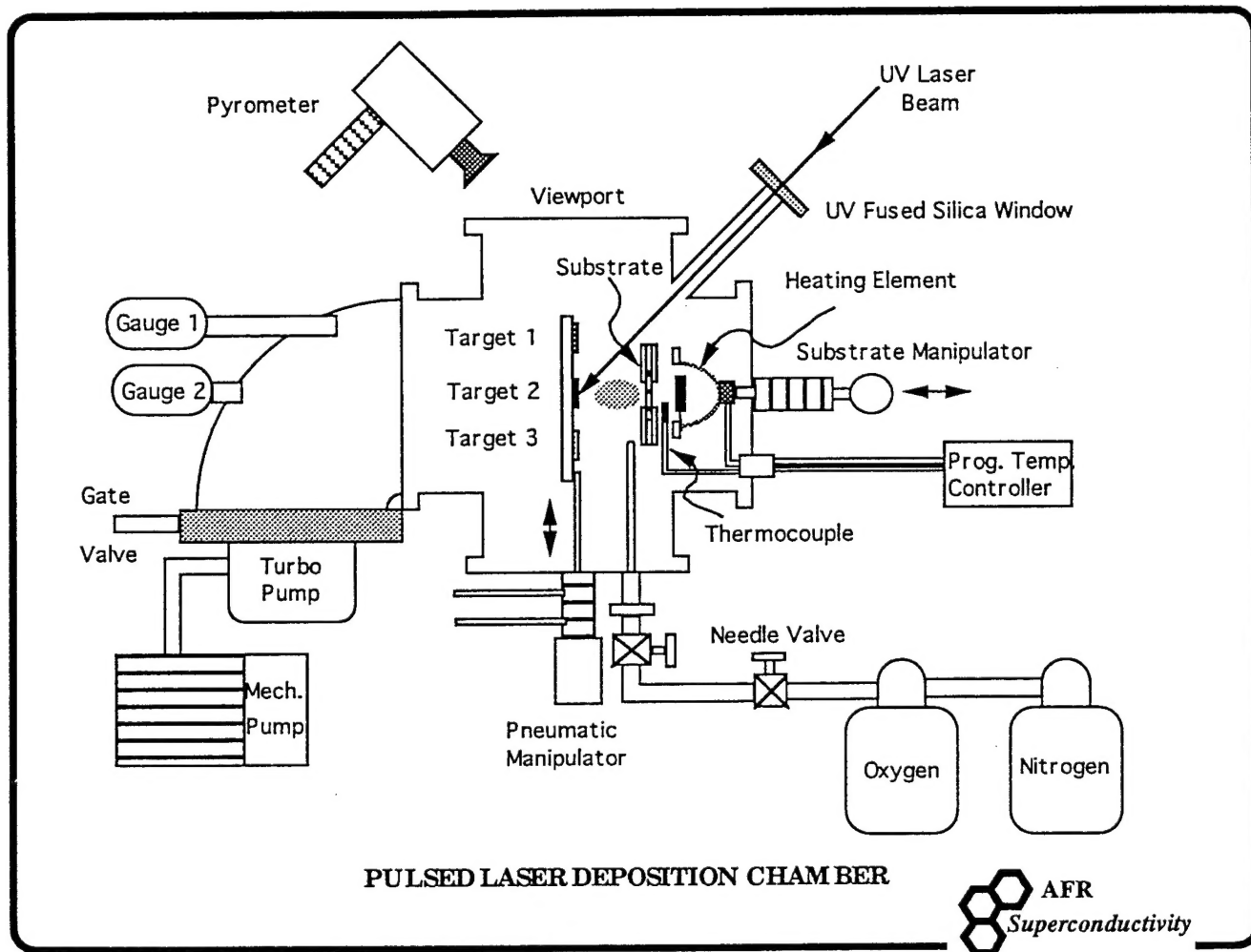


Figure 3. Schematic view of the pulsed laser deposition (PLD) system at AFR, Inc.

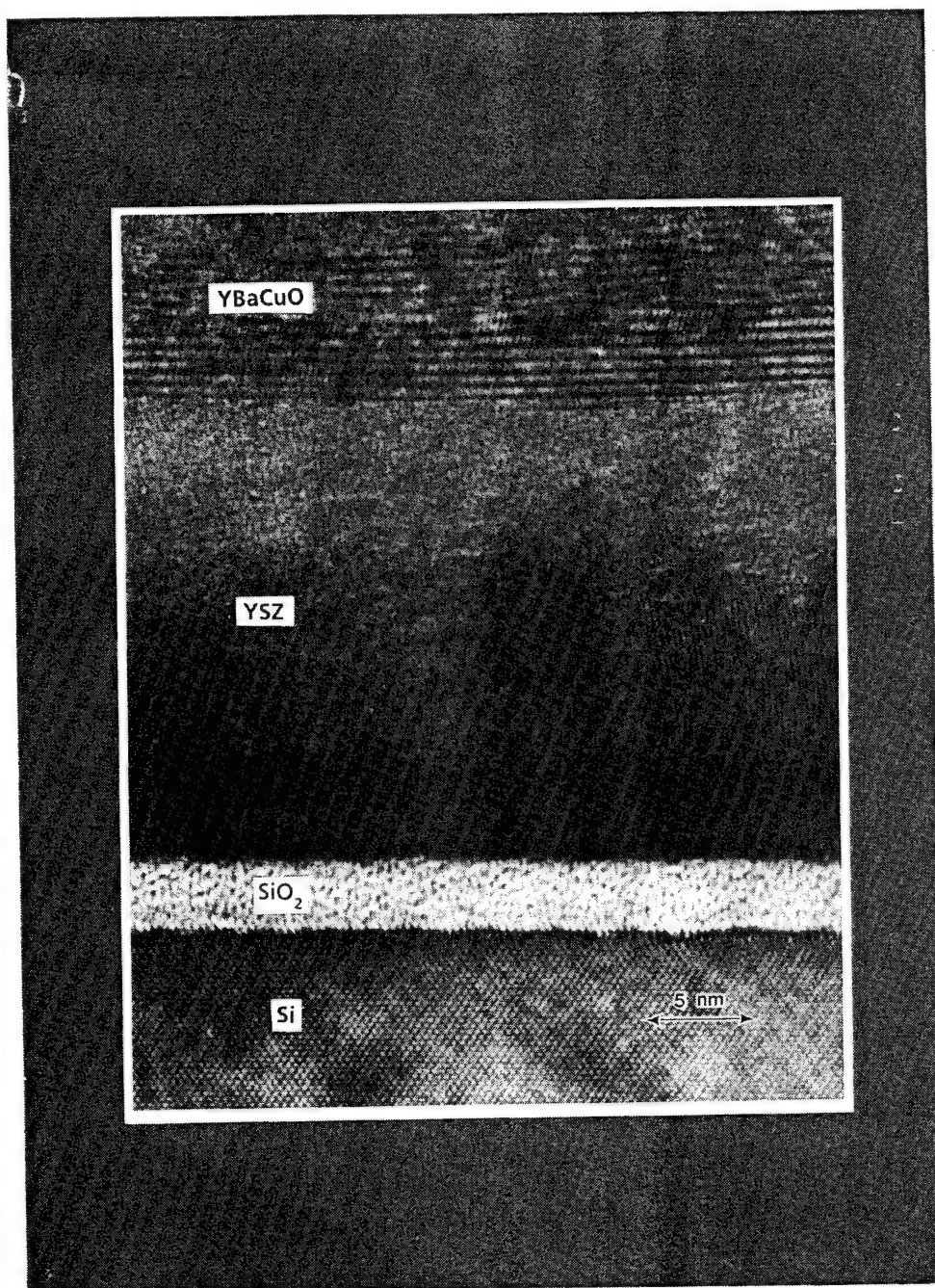


Fig. 4. Cross section transmission electron micrograph image of a YSZ buffered film of YBCO grown on a silicon substrate.

Because of the wide range of applications possible and frequencies accessible with Josephson devices, the properties of the substrates from dc through the infrared are of interest. We have demonstrated that the commercial (CZ) silicon wafers on which we grow our YBCO films are transparent to IR through a wide wavelength range. For these wafers, carrier freeze out by 90 K greatly lowers the free-carrier optical conductivity in the mid- to far-IR range, and the only significant infrared absorptions are the relatively narrow multiphonon and impurity local vibrational mode absorption bands. Transmission measurements on various competing substrates for YBCO film growth, have been made, and only silicon is useful across the mid- and far-IR range [17]. These IR measurements were done in collaboration with Prof. H.D. Drew's group at the University of Maryland. They found that the substrates provided such an unobstructed view of the IR transmission of very thin YBCO films, that several new IR features of the YBCO could then be easily observed. This in turn lead to the rapid publication of two important articles [18,19].

The use of HTS thin films in passive microwave components is current being pursued in many R&D centers, primarily with the use of LaAlO_3 substrates. In microelectronics, silicon wafers are the best choice of substrate for many technological reasons related to their vast use, but for HTS applications in the microwave through infrared wave ranges, little is known.

2) HTS Josephson Junctions:

Unlike the situation with thin films, to the best of our knowledge an HTS Josephson technology compatible with silicon substrates has not been demonstrated before this program. There have been true breakthroughs, though, in the fabrication of Josephson junctions on metal oxide substrates[3,4,7]. As we will see for the junction technologies explored in Phase I, none of these breakthroughs depend in any crucial way on the exact nature of the substrate material, other than on its ability to support the necessary epitaxial film growth and ancillary processing.

A generic Josephson junction consists of two superconducting electrodes connected weakly by an extremely thin barrier. The HTS junction barriers of relevance to us are composed of either a thin bridge of a normal metal such as gold or silver [3-5], or by a defective (nonsuperconducting) material derived from the superconductors themselves [7, 9]. Both barrier types have yielded devices with excellent electrical properties on oxide substrates, and the Phase I results on silicon substrates were essentially the similar. We will describe Josephson junction fabrication briefly here, more details of our approach for silicon substrates are presented in section 3.

Step Edge SNS junction Fabrication-

This fabrication method was originally developed for oxide substrates such as that used by the P.I. and co-workers in previous studies[3, 5, 11]. Fig. 5 shows a schematic of the process sequence. First, nearly vertical steps are fabricated in the substrate using an anisotropic etch. The edges are defined using either a photoresist or a conformal metal mask as an etch stencil. After etching, the mask is removed and a YBCO film is grown on the substrate from roughly a 45° angle of incidence. The shadowing effect of the substrate step causes an electrical break in the superconductor. Without breaking vacuum, the substrates are rotated and a noble metal (Au, Ag or AgAu alloy) film is deposited so as to fill in the break between the superconducting electrodes, forming the microbridge. Because the bridge length is determined mainly by the step height and the YBCO thickness, excellent process control down to extremely short bridge lengths (~ 20 nm) is possible. After the films are deposited, the wiring and junction widths are defined by a wet or dry etch. An optional final etch to reduce the overlap area between the noble metal films and the top surfaces of the superconductors can be employed to reduce the parasitic shunt conductance [3]. This has the effect of raising the $I_c R_n$ product (characteristic voltage) of

the junction, increasing its speed, power handling, and signal to noise capabilities.

Step edge SNS junctions of this type on oxide substrates have been reported with record breaking frequency response and voltage swing[3,8,10]. Work by the P.I. demonstrated the ac Josephson effect (Shapiro steps) out to at least 8 THz using rf signals ranging from microwave frequencies up to 1 THz. The observed junction characteristic voltages were greater than 10 mV. These are the highest characteristic voltages and frequencies ever reported for the ac Josephson effect. The results establishes the vast frequency range accessible by HTS Josephson RF devices. These numbers are approximately a factor of 10 better what had been achieved previously with HTS materials.

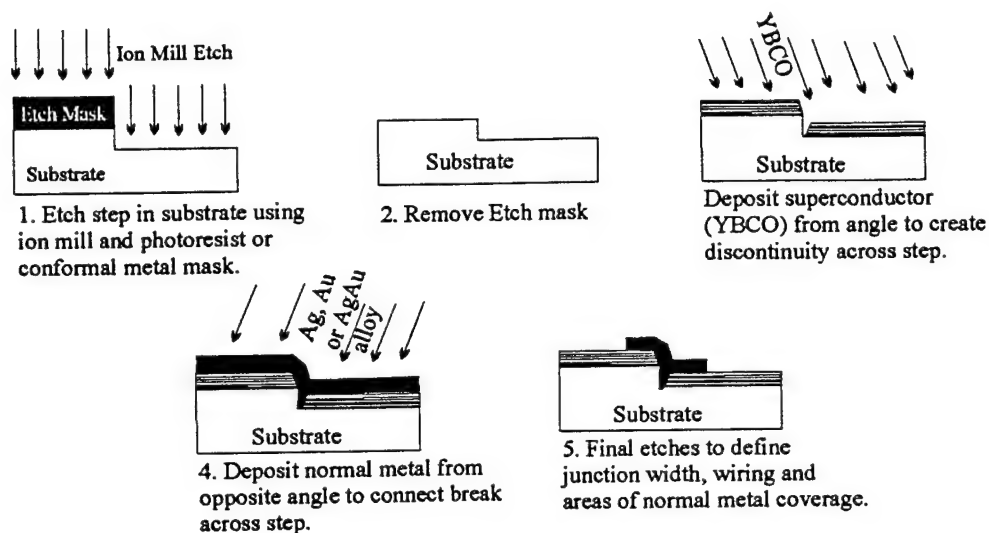


Figure 5. Process sequence for fabrication of step-edge SNS Josephson junctions.

Electron beam modified Josephson junctions

Unlike step edge SNS junctions, these devices are fabricated on planar substrates and require minimal substrate processing. Electron beam modified microbridges have been studied on oxide substrates by two groups [7, 9]. The basic idea behind this approach is to use a finely focused electron beam to generate a nanometer scale region of damage (weakened superconductivity) in the HTS film, thus forming a barrier separating the two superconducting electrodes. If the length of the weakened region is comparable to or smaller than the superconducting coherence length then Josephson coupling may be observed between the superconducting electrodes. For these electron beam damaged structures, the precise nature of the modified region is not well understood. Work at Cornell suggests that localized oxygen deficiency or disorder plays an important role in producing the weak link[20]. In spite of the uncertainty about the basic mechanism in these devices, they work quite well. Gurvitch et al have reported excellent electrical properties for bridges modified by a scanning Transmission Electron Microscope (STEM)[7]. Critical currents of ~ 0.3 mA and device resistances of order 1Ω at 77 K were achieved, with critical current and

resistance uniformities around 20 %. These junctions do not require any special substrate properties other than the ability to support high quality epitaxial growth, and in Phase I we exploited this technique to fabricate working junctions on silicon substrates.

HTS rf Devices:

The advantages of using superconducting thin film passive components for rf applications are well known[1, 2]. Substantial gains in weight, insertion loss and Q can be obtained when the normal metal conductors used in microwave coplanar waveguide (CPW), stripline and microstrip circuits are replaced with low loss HTS thin films. The performance gains come from two unique properties of superconductors 1) the extremely low surface resistance at microwave and millimeter wave frequencies, and 2) the nearly dispersionless propagation possible for signals along properly designed superconducting transmission lines. Both of these properties are advantageous for high speed and rf electronics. The low surface resistance of HTS films, however, is in many cases offset by deficiencies of the substrates. In this regard, the metal oxide substrates are typified by large and temperature dependent dielectric constants and loss tangents. Strontium titanate is a particularly pernicious material with an extremely temperature dependent dielectric constant over 300 at microwave frequencies. Lanthanum aluminate is more attractive, with a dielectric constant of 24, however the tendency of lanthanum aluminate to form crystallographic twin boundaries results in spatial variation of device properties across a chip. These effects can limit the Q values and cut-offs attainable with high performance resonators and filters[2]. Furthermore, from a mechanical and processing point of view the oxides are especially difficult to work: large high quality wafers are not easily fabricated, they are difficult to thin and polish, and they often break during processing. In contrast, silicon is cheap, (even at 200 mm sizes) mechanically strong, lower in loss and dielectric constant than the metal oxides at cryogenic temperatures, and can be routinely thinned to micron thicknesses. The combination of HTS films and silicon substrates can result in the following improvements:

- Lower cost, better manufacturability than other substrates
- Compatibility with semiconducting active components
- Nearly dispersionless transmission lines to THz frequencies
- More compact delay lines (and longer delays)
- Suppression of unwanted (non TEM) transmission line modes at higher frequencies
- Higher Q resonators and sharper filter cutoffs
- Lower insertion loss

At present, HTS films on silicon must be kept to 70 nm thickness or less to prevent cracking caused by the mismatch in the film and substrate thermal expansion coefficients. This constitutes a technical hurdle to achieving the lowest possible values for the surface resistance. For the lowest values of R_s , the optimal film thickness is greater than the penetration depth, about 200 nm at 77 K for high quality films. As we stated in section 2, one of the goals of the Phase II program will be to demonstrate a new compliant substrate technology to allow growth of high quality, low stress HTS films of arbitrary thickness on silicon. *If successful, this will be a major breakthrough for rf applications of HTS thin films.*

RF Josephson devices - The study of active i.e. Josephson superconducting elements for rf signal processing has a long history[21,22]. LTS Josephson junctions have been shown to be excellent mixers, but the full potential of HTS Josephson junctions as nonlinear elements has yet to be practically demonstrated. Most rf applications of the Josephson effects involve junctions serving as nonlinear elements coupled to passive structures such as delay lines, filters, resonators and transmission lines. The

combined properties of junctions and passive structures on silicon substrates at microwave and millimeter wave frequencies are therefore of primary interest, and it is essential to have a useful equivalent circuit model for design purposes. Tasks 2 and 3 of the Phase I program addressed this issue by demonstrating that the observed junction dynamics were well described by the resistively shunted junction (RSJ) model [23, 29].

3. TECHNICAL RESULTS

3.a. Task 1 - Junction Fabrication

Objective

To fabricate Josephson junctions with properties tailored for rf applications on silicon substrates.

Results

In Phase I we developed fabrication processes for 1) Step edge SNS Josephson junctions on silicon, and 2) Electron beam modified Josephson junctions on silicon.

3.a.1. Step edge SNS Josephson junction fabrication

Process Overview -

The fabrication process developed in Phase I was composed of three separate steps 1) Step edge fabrication, 2) Film deposition, and 3) Junction definition by lithography. These steps are illustrated schematically in Fig. 6.

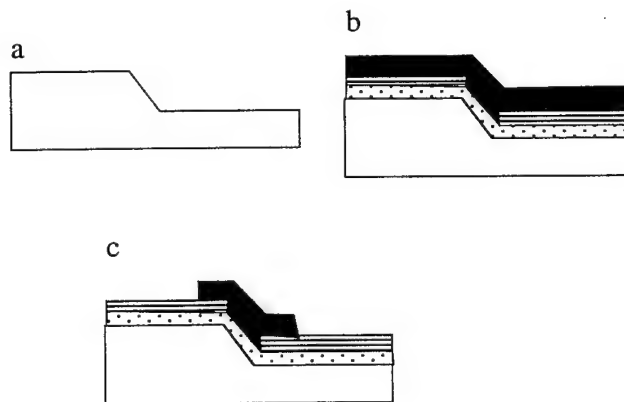


Fig. 6. Process sequence to fabricate step edge junctions on silicon: (a) fabricate step edges, (b) HF passivation and film deposition, and (c) junction definition by photolithography and ion milling.

1) Step Edge Fabrication

One of the objectives of this program was to explore the rich variety of available techniques to fabricate step edges in silicon. In Phase I we explored three methods: (wet) anisotropic etching, argon ion milling, and reactive ion etching (RIE). After etching steps using the three approaches, we judged that reactive ion etching was the most promising method for phase I, combining the virtues of reasonably good step morphology, repeatable fabrication, and minimal damage to the etched silicon surface. We note, though, that the other methods also have merit, and further work is justified to fully assess the potential of the different step fabrication processes.

Wet Anisotropic etch: It is well known that a KOH solution is an excellent anisotropic etch for silicon, with a high etch selectivity of the (100) direction as compared to the (111) direction. An etch at a boundary parallel to a (100) direction will therefore result in a sloped step of approximately 54° relative to the (100) surfaces. The step itself will be a (111) facet. This method of forming three dimensional structures has been widely studied in the context of fabricating micro-electromechanical structures (MEMS), but has not been examined for step edge Josephson junction fabrication. In Phase I, we fabricated step-edges in silicon using a wet KOH anisotropic etch. The pattern was defined by a thermal oxide mask, which was itself patterned photolithographically, and etched with a buffered oxide etch. We found the etch rate and film morphology to vary strongly with etch parameters, and the etched surfaces were generally extremely rough. We attempted to improve the quality of the surfaces and steps by employing combinations of different surface treatments, including spin-etching with HF, various agitation levels including ultrasonic and magnetic stirring, and etch temperatures ranging from 20°C to 55°C . In all cases the etched surfaces were rough. As the temperature was increased, the etch rate became more unpredictable. After these experiments, wet etching was abandoned as a means of step fabrication for Phase I. Fig. 7 and Fig. 8 compare atomic force microscope images of a KOH etched to an RIE step described below. As can be seen, the two steps and the surface morphology appear quite different. Notice that the step etched in 55°C KOH is smoother than the RIE step shown in Fig. 8, but the surface morphology is rougher. If this process can be improved, it may well yield better and more reproducible junctions than the RIE based process. Unfortunately, the limited results of the Phase I effort were that the etch rate was difficult to control, and that the wet etched silicon surface was rougher than ion milled or RIE processed surfaces. In our opinion, more work in this area is justified, and should be pursued in Phase II.

Ion Milling: The NIST group has been using ion-milling routinely to fabricate step-edges in lanthanum aluminate substrates. They were successful in fabricating sharp (approximately 80°) steps in silicon by this method, however, the surface damage from the ion beam prevented the subsequent growth at NIST of superconducting YSZ buffered YBCO on the etched surface. Because these steps were so sharp, however, we believe that more experiments to improve the surface properties should be carried out in Phase II. In particular, we believe that a high temperature anneal ($\sim 1200^\circ\text{C}$) in hydrogen would reconstruct the silicon surface as well as remove any native oxides. Ion milled steps in silicon with improved surfaces might then yield significantly better junctions with much higher yield.

Reactive Ion Etch: Using the sulfur hexafluoride (SF_6) reactive ion etcher at NIST, we were able to fabricate sharp reproducible steps of approximately 100 nm height and 60° slope in silicon substrates. The RIE process parameters are summarized below and an AFM image of a typical RIE processed step is shown in Fig. 8. The success of this method is particularly encouraging, because of all the step fabrication techniques explored in Phase I, RIE is the most production compatible method. Unlike ion-milling, reactive ion etching is readily adapted to large areas and multiple wafer batches. It is

also extremely fast, repeatable, and relatively gentle to the etched silicon surface. As we will see, the surface left by the RIE process was capable of supporting subsequent growth of epitaxial YSZ and YBCO after a clean and spin-etch cycle. The etch recipe is summarized in Table 1.

RIE Process Parameter	Value
Sulfur Hexafluoride (SF ₆) flow	30 sccm
Oxygen Flow	10 sccm
Pressure	10 mT
Bias Voltage	-60 V
RF forward power	25 W
RF reverse power	2 W
Time	90 s
Total Depth Etched	95 nm
Etch rate	1.06 nm/s

Table 1. Reactive ion etch recipe developed to fabricate step edges in silicon.

Fig. 8 shows an AFM image supplied by NIST of a typical RIE processed step in a silicon substrate. Note that although the RIE formed step is somewhat rougher than the KOH etched step in Fig. 7, the etched surface of the substrate is significantly smoother.

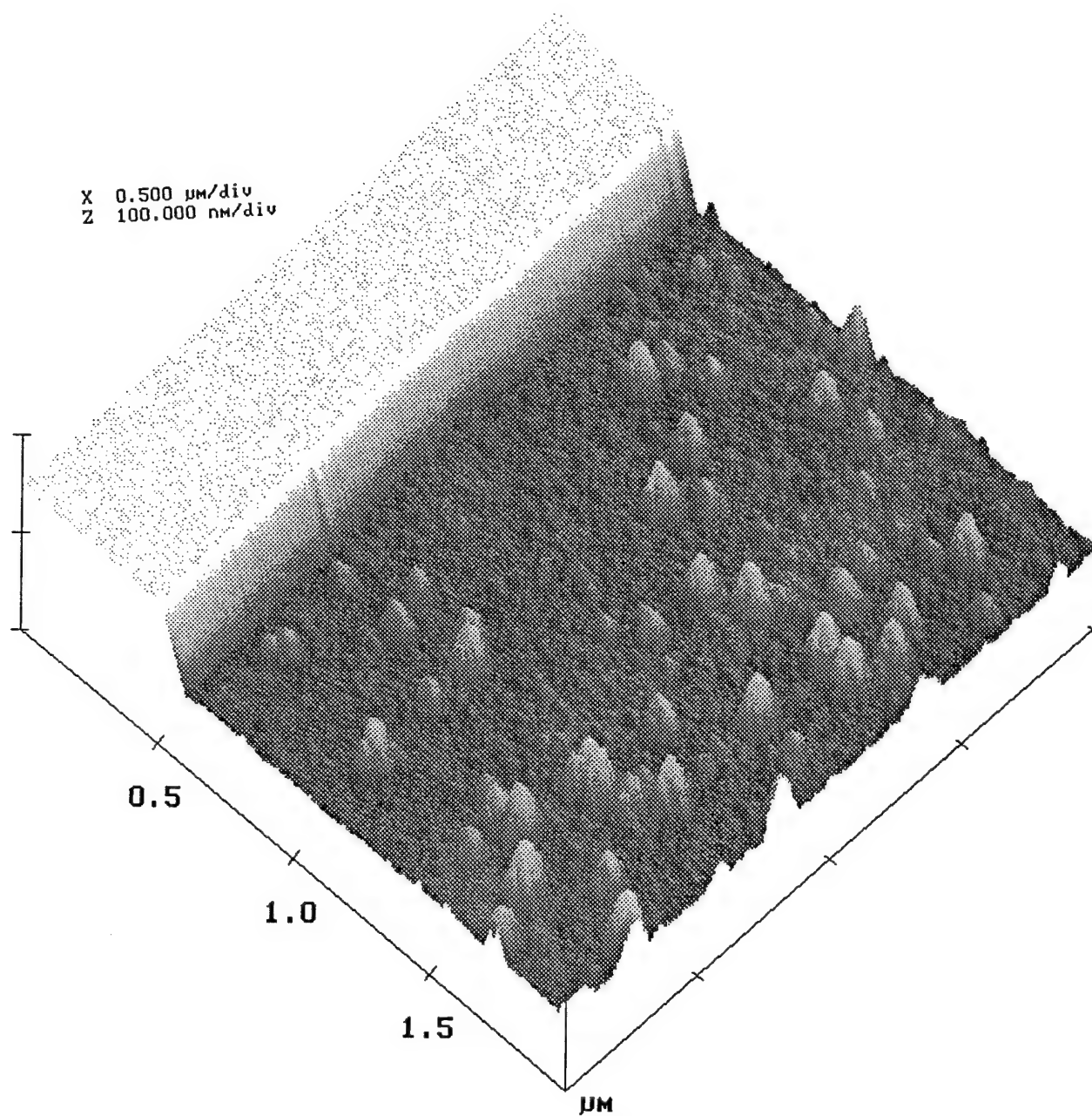


Fig. 7 Atomic force microscope image of step edge fabricated 55 °C KOH etch.

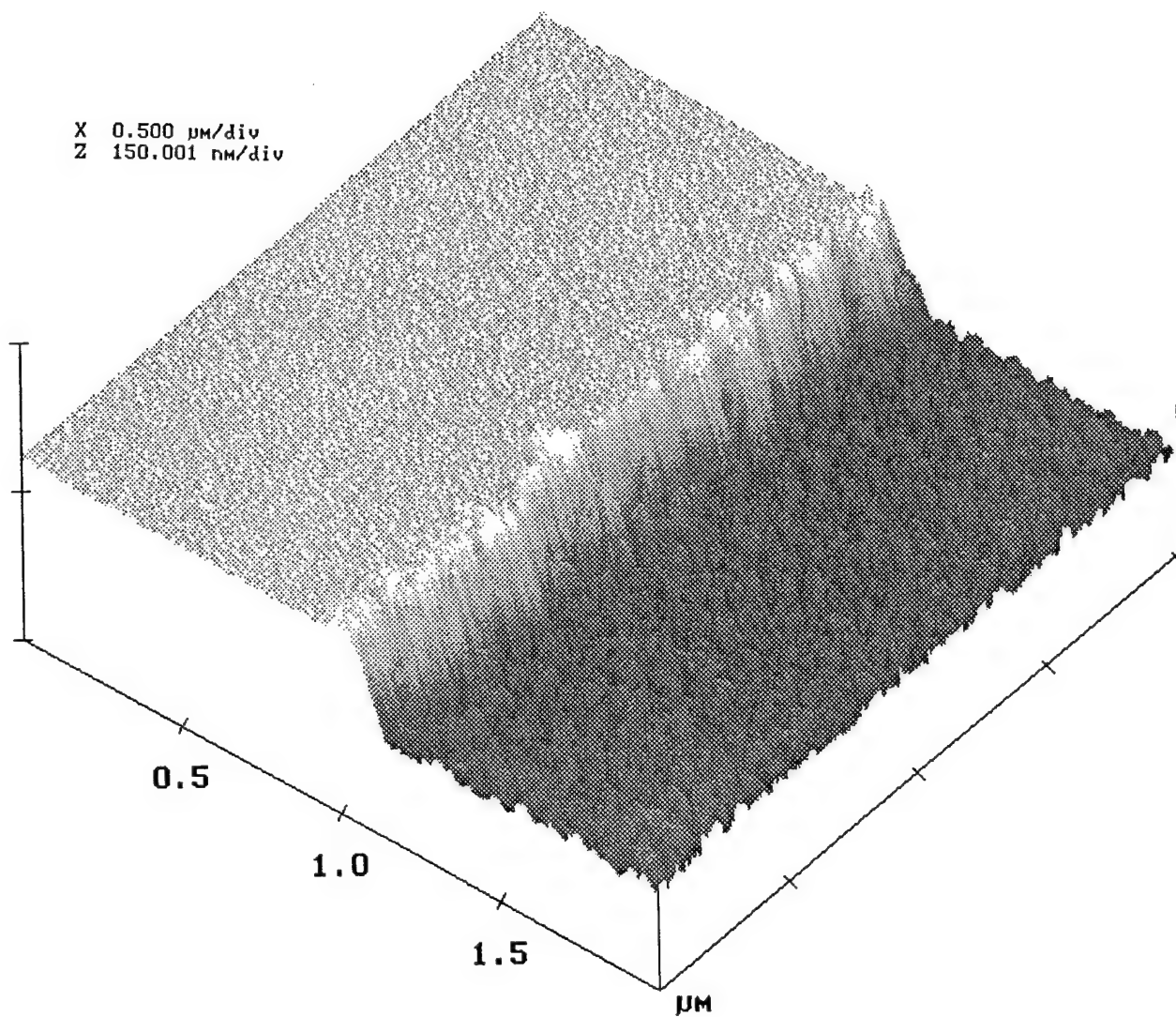


Fig. 8. Atomic force microscope image of step edge fabricated by reactive ion etching.

Film Growth

After the steps were fabricated, the wafers went through solvent cleaning and HF passivation. Next, the YSZ buffer, HTS and gold layers were deposited. The original plan in the proposal was to have the films grown at NIST, because they already had a PLD facility capable of performing the required angled depositions of the various layers. Unfortunately, within the time constraints of the Phase I program, they were not able to grow crack-free films thicker than about 20 nm, nor were they able to grow films with good properties on reactively ion etched surfaces. Figure 9 (a) shows an SEM photo of a typical NIST film grown on a pristine silicon substrate. As the figure shows, the film is riddled with cracks along the (100) directions. Fig. 9 (b) shows a film grown by AFR. The morphology is clearly different, and while there are some irregularities to the surface and some outgrowths, there is no evidence of stress related cracking.

Figs. 10(a) and 10(b) compare the surfaces of films grown at NIST and AFR on reactively ion etched substrates. Notice how the NIST film (Fig. 10(a)) is riddled with holes while the AFR film is comparatively continuous. After experimenting with the deposition temperature and cleaning procedures without success, we dropped the plan to grow the films at NIST and prepared to perform the angled depositions at AFR. Thus we added a task to the program to build a new substrate furnace at AFR that would allow deposition over a ± 50 degree angular range and grew the junction films at AFR.

The AFR Rotatable Substrate Heater

Photographs of the new furnace are shown in Fig. 7. The new furnace was capable of heating 12 mm square substrates identical to those used at NIST to over 1000 °C. The furnace used a silicon carbide heating element to heat the substrates radiatively from behind. The substrate temperature was monitored with a pyrometer. The entire assembly was well shielded to maximize radiative efficiency. The furnace was mounted on a gimble, and articulated for rocking with a miter gear and graduated rotary feedthrough. A thermocouple mounted behind the silicon carbide element provided an additional independent (but indirect) temperature measurement.

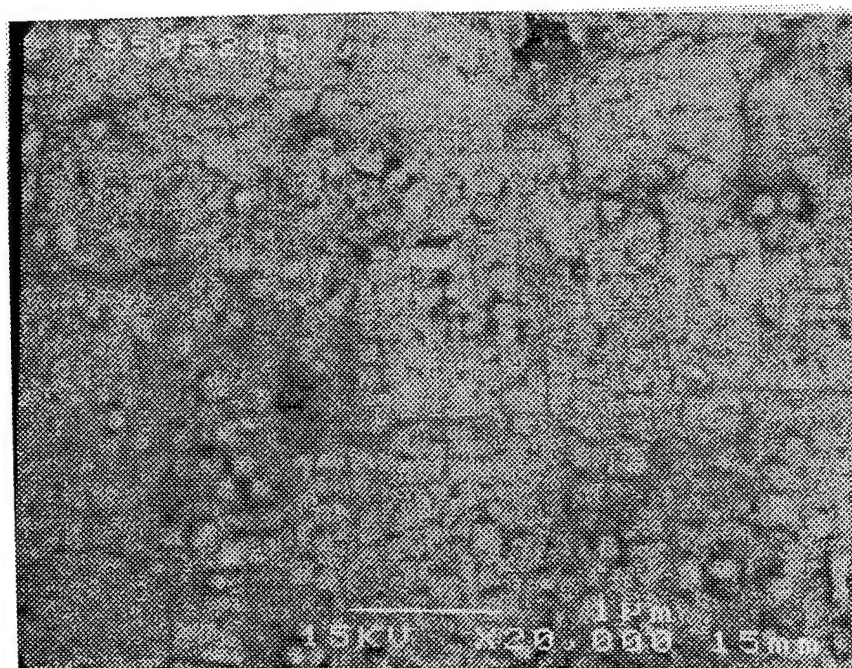
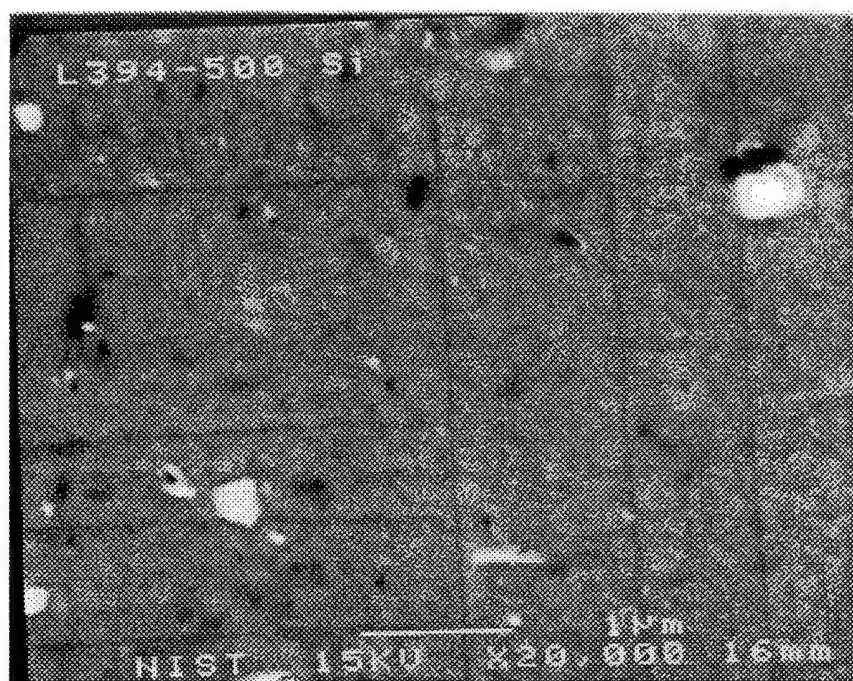


Fig. 9. SEM images of (a) 50 nm thick HTS film grown at NIST on RCA-cleaned silicon substrate using the KrF excimer laser, and (b) 50 nm thick HTS film grown at AFR on HF passivated silicon substrate using a quadrupled YAG laser.

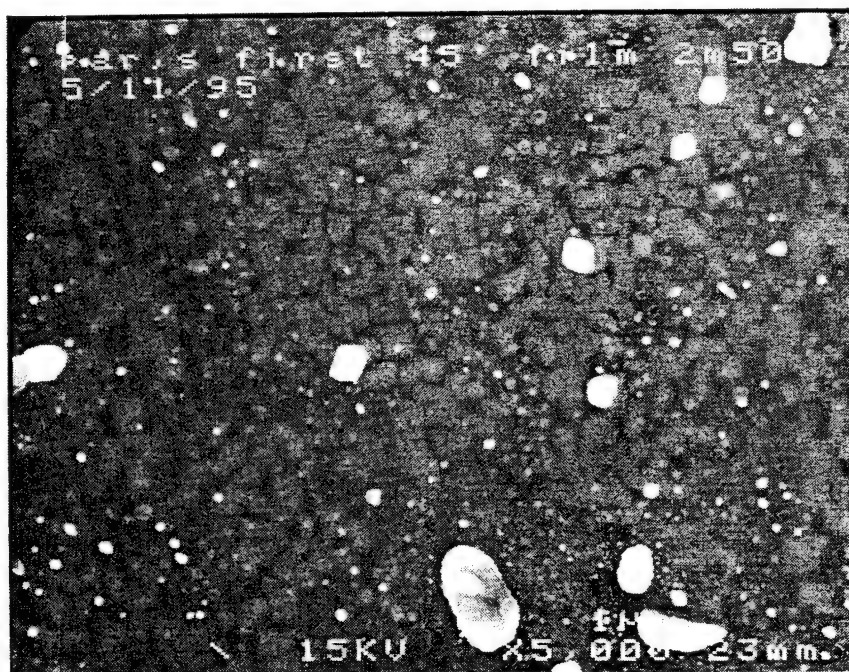
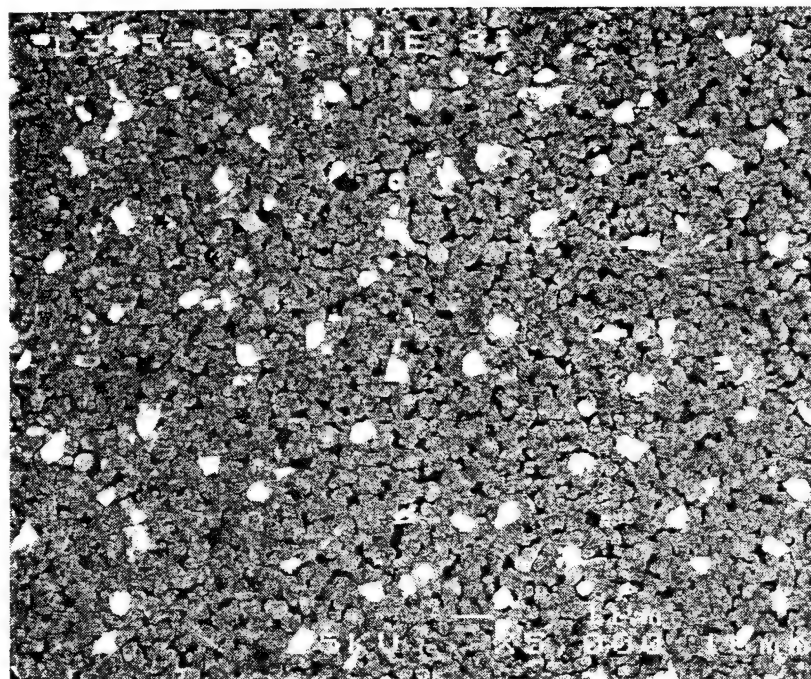


Fig. 10. SEM images of (a) 50 nm thick HTS film grown at NIST on RIE processed silicon substrate using the KrF excimer laser, and (b) 50 nm thick HTS film grown at AFR on RIE processed silicon substrate using a quadrupled YAG laser.

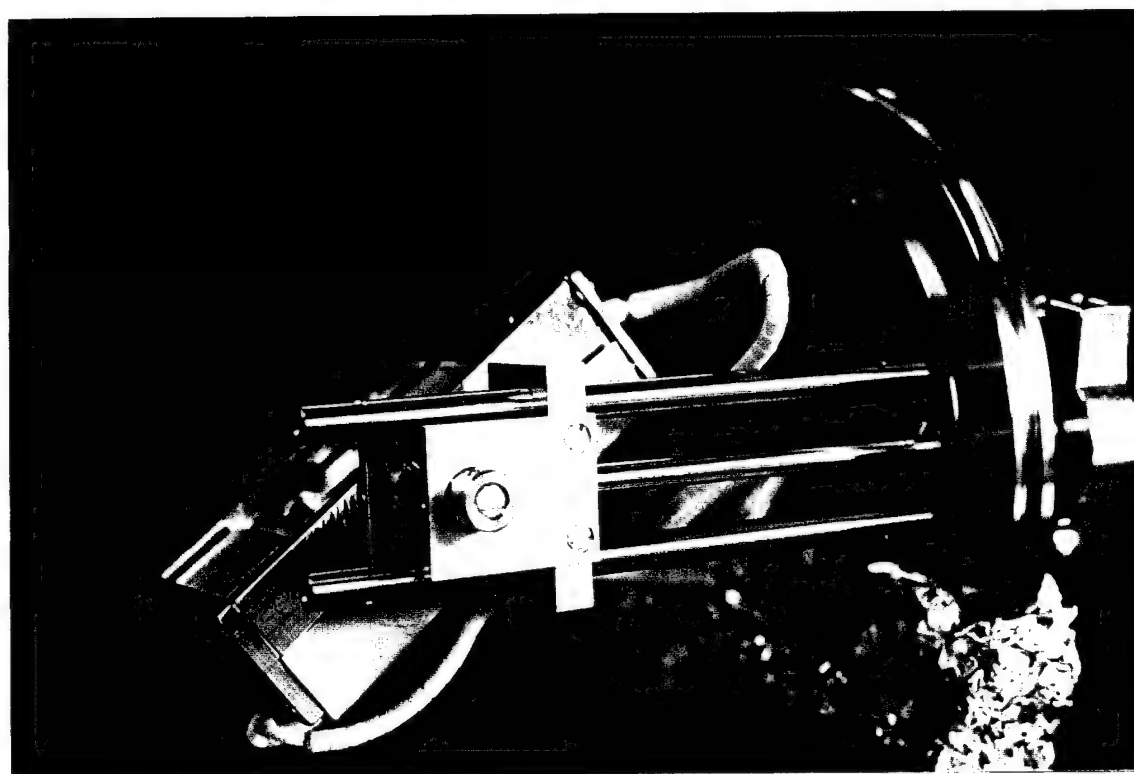
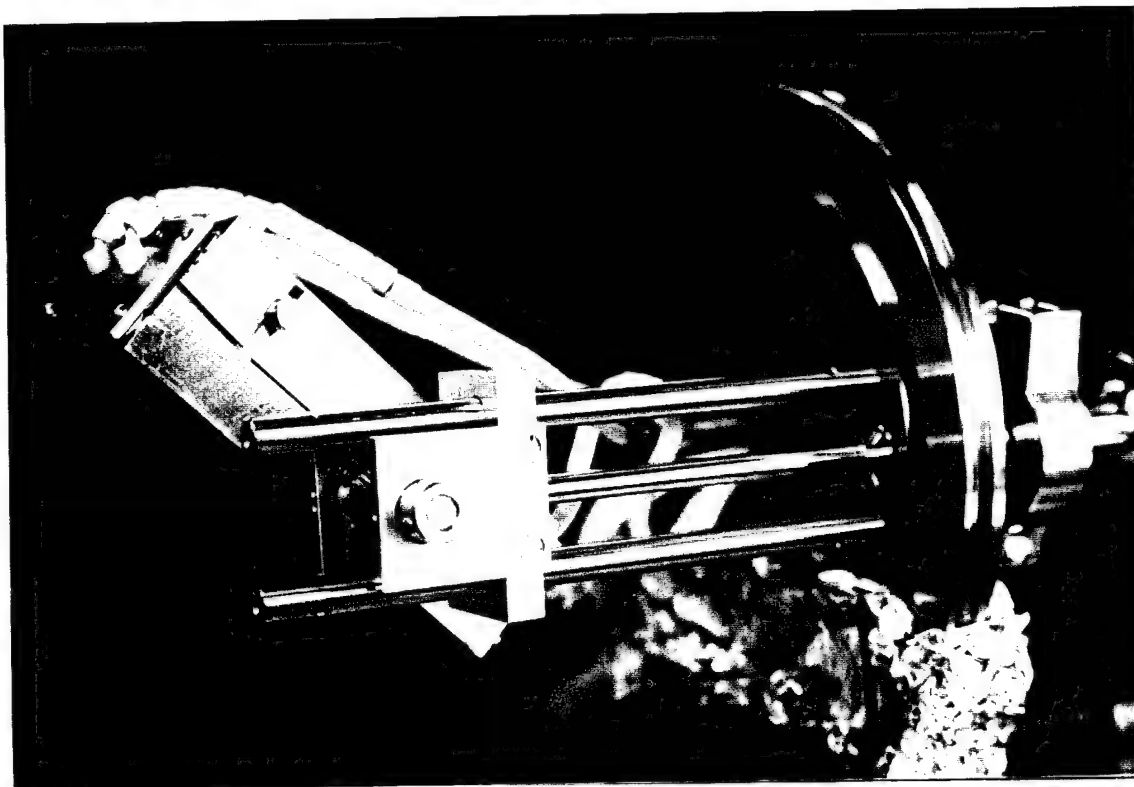


Fig. 11. Photographs of the AFR rotatable furnace showing the extended range of angular motion.

Growth of HTS films on reactive ion etched surfaces is not trivial. As we have already shown, NIST was not able to grow high quality films on the etched surfaces. In contrast, after an HF spin-etch surface treatment, we were able to grow superconducting films on the etched surfaces at AFR. It is unclear why AFR had better success with these substrates. The two most significant differences between the NIST and AFR processes are deposition lasers and the surface cleaning treatments. AFR uses a 260 nm quadrupled YAG laser with a fluence of about 1.5 J/cm^2 on a beam spot about 1 mm^2 . NIST in contrast uses a 248 nm KrF excimer laser with a fluence of around 2 J/cm^2 , but with a much larger beam spot ($\sim 3 \text{ mm} \times 5 \text{ mm}$). The overall growth rate at NIST is much higher. NIST does not routinely passivate the silicon surface before growth, and their substrate heating and cooling are much slower than at AFR.

Film deposition for junction fabrication

The film deposition sequence for junction fabrication is shown schematically in Fig. 12. Before mounting in the deposition chamber, the substrates were cleaned and then passivated with an HF spin-etch.

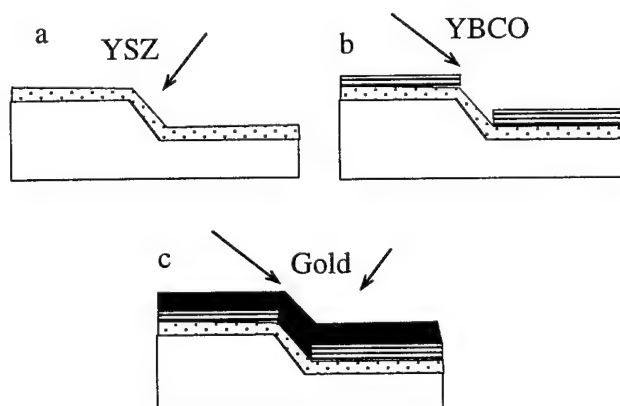


Fig. 12. Film deposition sequence for step-edge SNS Josephson junction fabrication on silicon.

YSZ deposition - The YSZ films were deposited at 800°C as determined by pyrometer, in 4×10^{-4} Torr O_2 . In earlier attempts to fabricate films on silicon step edges, it was noted that the growth morphology at the step depended on the incidence angle of the YSZ buffer layer [24]. When the was deposited to form a break at the step, then large outgrowths and irregular structure marked the step edge. When the YSZ was deposited into the step as in Fig. 12 (a) then there was less of a tendency to form outgrowths at the step edge. We repeated this experiment with films grown at AFR. The results are shown in Figs. 13 and 14. Fig. 13 is a photo of a step in which the YSZ was deposited over the step. Fig. 14 shows the case were the YSZ was deposited into the step. In both cases the subsequent YBCO layer was deposited over the step as in Fig. 12 (b). The film morphology at the step edge appears cleaner in Fig. 14, however the effect is not as strong as was previously observed at NIST. More work remains in this area.

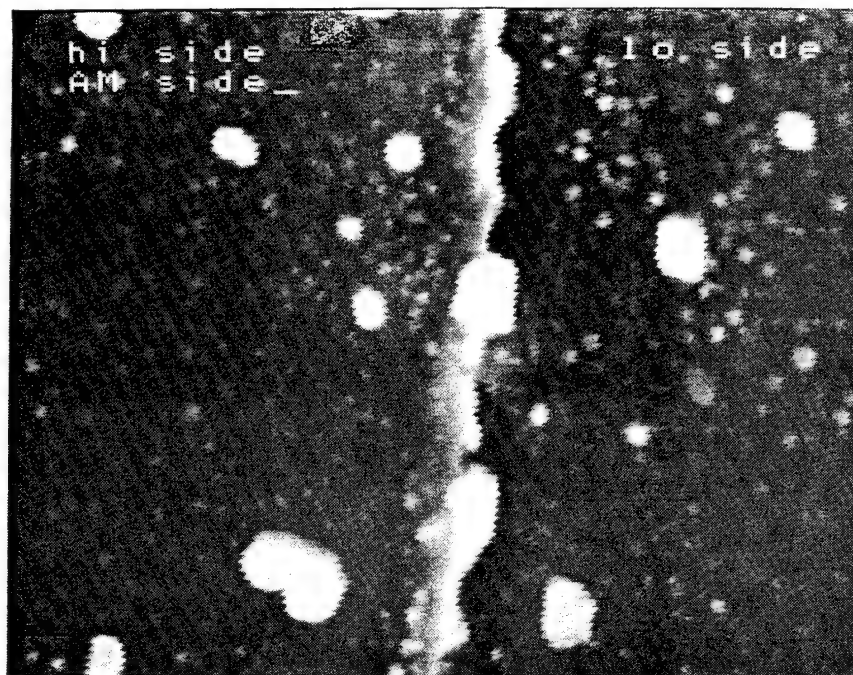


Fig. 13. YBCO growth at step when the YSZ buffer layer is deposited over the step.

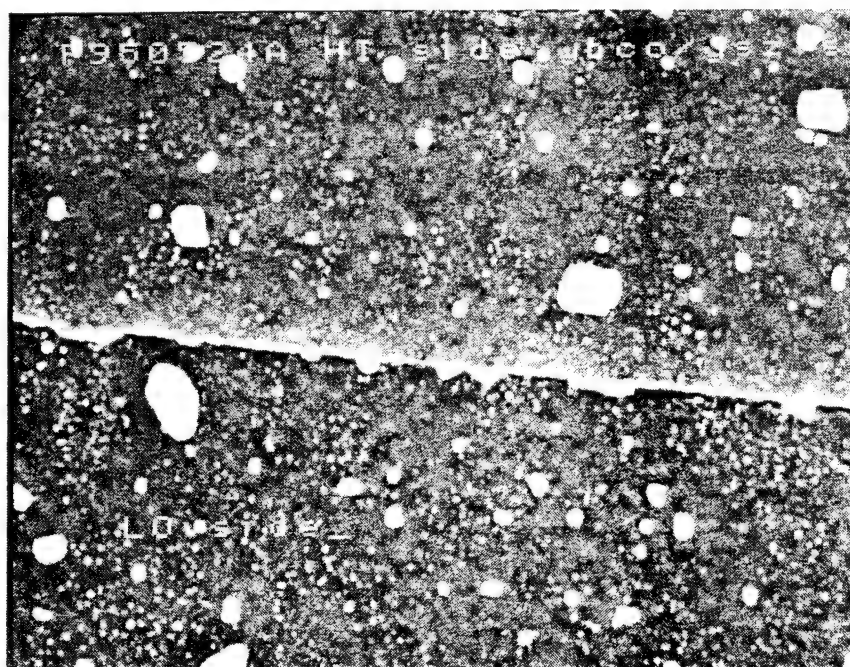


Fig. 14. YBCO growth at step when the YSZ buffer layer is deposited into the step.

YBCO deposition - After the YSZ deposition, without breaking vacuum, the substrates were cooled to 780 °C, and the chamber was backfilled to 200 mTorr O₂. The YBCO was then deposited at a 50 degree angle of incidence so as to form a break in the shadow of the step (Fig. 12(b)). After the YBCO was deposited, the samples were cooled in oxygen.

Gold Deposition - When the samples had cooled to near ambient, the chamber was pumped out and backfilled to 50 mTorr O₂, and the gold was deposited to form the junction as in Fig. 12 (c). Background gas is required for PLD growth of gold because in vacuum the plume actually etches the growing film faster than it lays the gold down. To improve step coverage, the gold was deposited from two directions: The first two thirds were deposited into the step, then the heater was rocked, and the last third was deposited over the step.

Junction Definition by Lithography

After the YSZ/YBCO/Au film stacks were deposited on the etched substrates, positive photoresist was spun onto the films, and they were patterned using photolithography and ion milling. Fig. 2 on page 6 shows the chip layout with a close-up of the junction area. The pattern included 14 independent junctions and one series array of 9 junctions. Each junction or the array could be measured by four point probing through the twenty-five contact pads on the chip. After ion-milling and stripping of the resist, the junctions were essentially complete and ready for testing.

3.a.2. Electron Beam Modified Junction Fabrication

Unlike the step-edge SNS process, the e-beam junction fabrication required only minimal substrate processing. The substrates were cleaned in detergent, trichloroethylene (TCE), acetone and alcohol. Immediately prior to mounting in the deposition system, the silicon chips were spin-etched in a buffered HF solution to remove the native oxide and passivate the silicon surface. The samples were then mounted in the PLD system. 50 nm of YSZ were deposited at 4×10^{-4} Torr oxygen, followed by 50 nm of YBCO at 200 mTorr oxygen. The samples were then cooled slowly, measured for R vs T, and sent to Professor Michael Gurvitch at Stony Brook for patterning and junction fabrication. At Stony Brook, the chips were patterned into 4 micron wide microbridge and SQUID patterns using photolithography and wet (dilute HNO₃) etching. The chips were then mounted in the CM-12 Phillips electron microscope for junction formation. The beam was scanned once across each bridge to form a weak link. The parameters of the beam were: energy E = 120 keV, spot size = 3.5 nm, beam current = 5 nA.

3.b. Task 2 - Electrical Characterization

Objective

To determine the basic electrical properties of the most successful junction fabrication runs.

Results

3.b.1. Electrical Characterization of Step-Edge SNS Junctions

DC Testing

Josephson Critical Currents - Several working junctions were studied on two chips. The critical currents ranged to $84 \mu\text{A}$. The yield for finite critical currents was less than 50% for these preliminary experiments, but given the large process parameter space and the limited time available for process optimization, we consider the work to be extremely successful. The junction with the highest critical current was selected for more detailed studies. Fig. 15 shows dc current voltage (I-V) curves at 4 K and 40 K. The data show clearly an RSJ like shape, with noise rounding (presumably thermal) at 40 K. Note also as expected that the critical current is reduced at higher temperature. Fig. 16 shows the measured critical current of this junction as a function of temperature. Although we have not fit this data quantitatively, this general shape of I_c vs T curve is expected when the junction is longer than the normal proximity length. Given that the step height for this junction was 120 nm, and the YBCO film was only 60 nm thick, this is not surprising. Similar results have been obtained on lanthanum aluminate substrates [25].

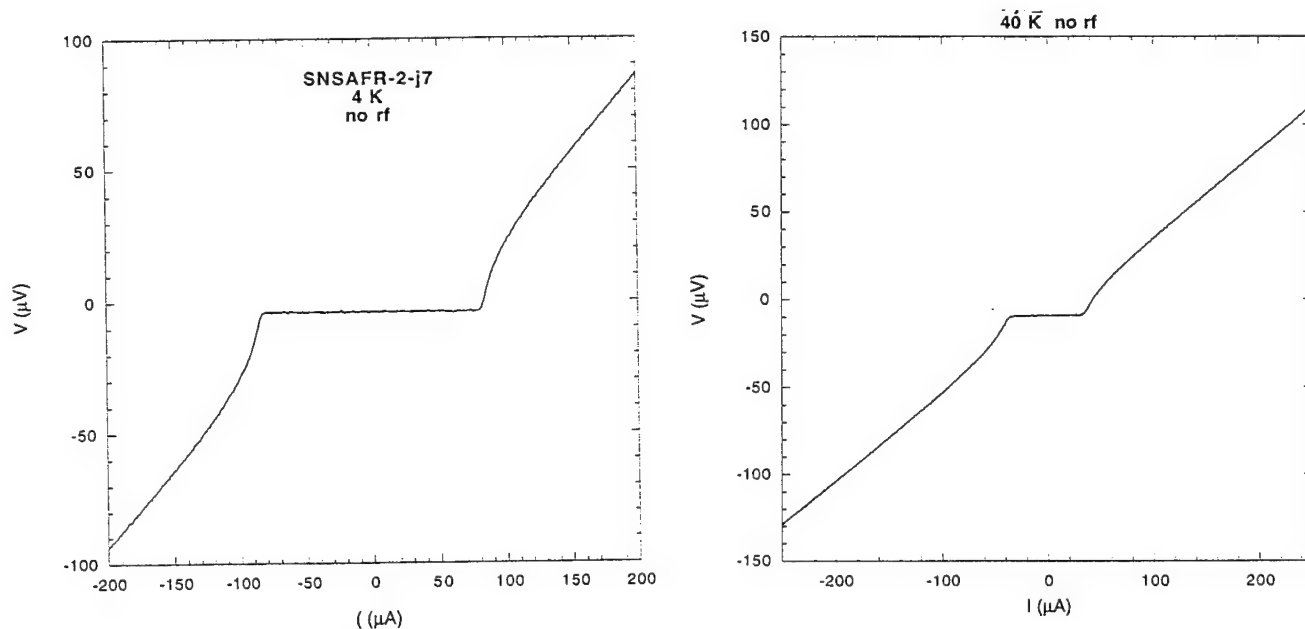


Fig. 15. Dc current-voltage curves at 4 K and 40 K for a step-edge SNS junction on silicon.

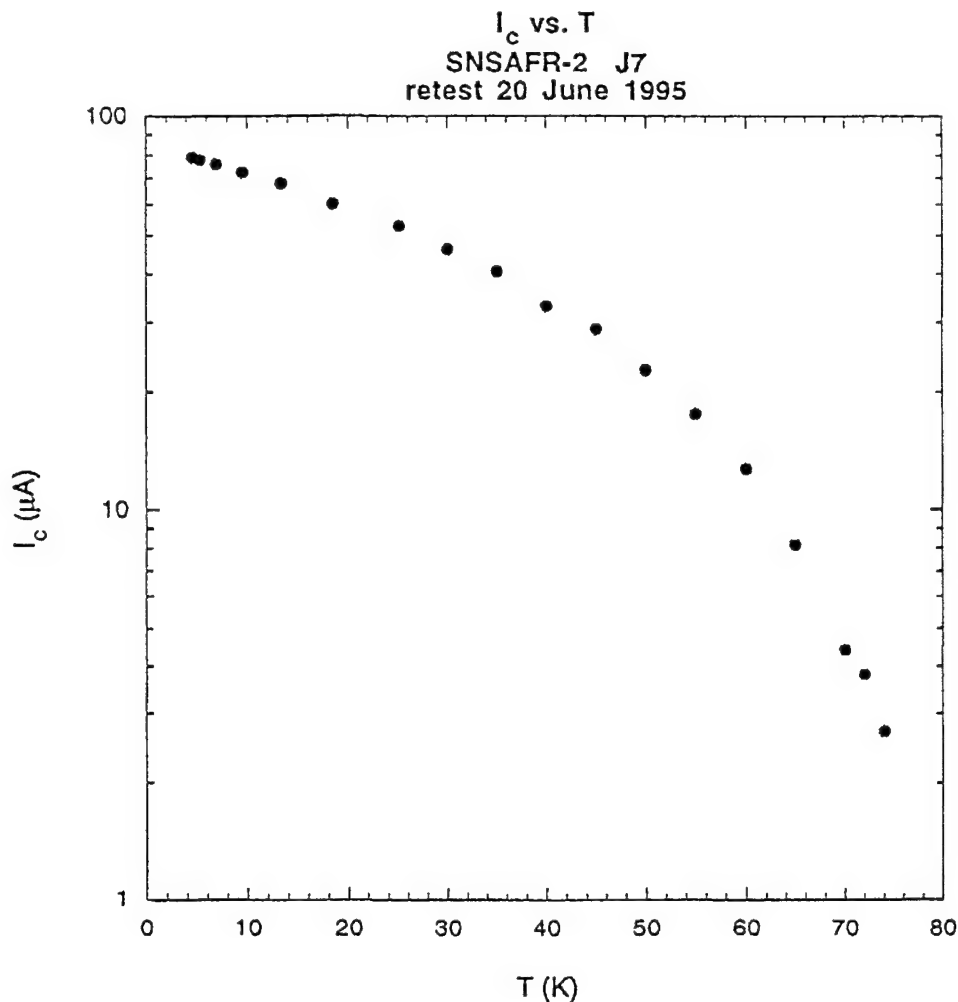


Fig. 16. Temperature dependence of the critical current of a step-edge SNS junction on silicon.

Grain Boundaries - In testing this chip, it was noted that if the bias current was raised high enough, then additional critical currents became evident. These were likely due to series grain boundaries or other weak links somewhere in the lead wires. Of the two chips studied with working junctions, it appeared that the grain-boundary effects were associated with the lower J_c part of the film that was deposited on the RIE etched surface. The chip with the higher critical current density on the etched surface exhibited wiring weak links only at much higher bias currents.

RF Testing -

8.3 GHz microwaves were applied to the junction during measurements at 4 K. At least 12 microwave induced Shapiro steps were clearly visible in the IV curve as shown in Fig. 17. **This implies a strong Josephson effect to at least 100 GHz.** As we will see in Task 3, there is every reason to expect good performance to even higher frequencies, based on the estimated capacitance, the junction $I_c R_N$ products, and a straightforward process modification to increase the junction resistance. We also measured and analyzed the power dependence of the microwave induced steps. These results are discussed in task 3 (section 3.c.)

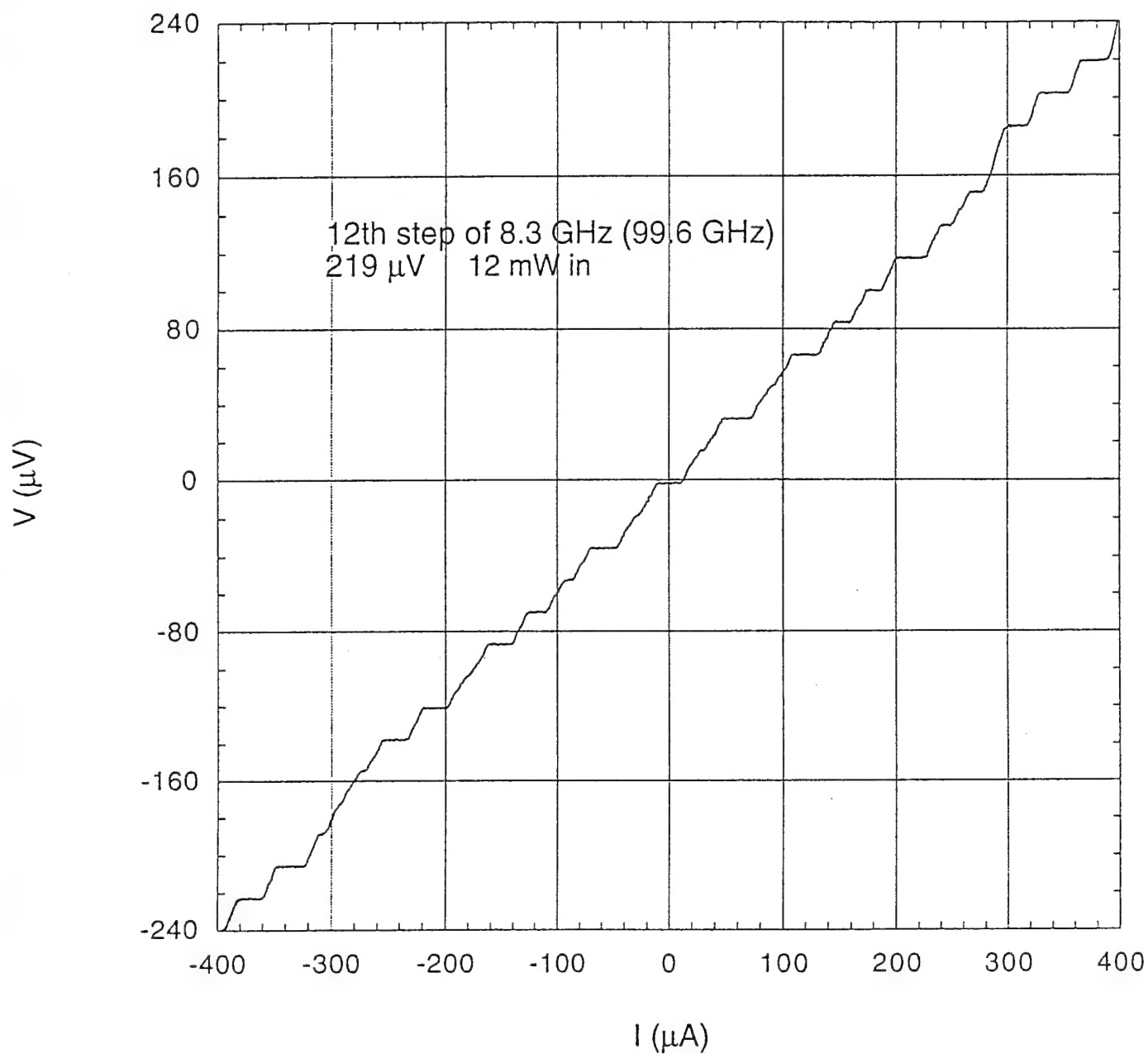


Fig. 17 Shapiro steps in a step-edge SNS junction on silicon. An 8.3 GHz microwave source was used to excite at least 12 well defined steps in the iv curve.

3.b.2. Electrical Characterization of Electron-Beam Modified Junctions

The e-beam modified junctions were usually fabricated in pairs in dc SQUIDs. An electron micrograph of a typical device is shown in Fig. 18.

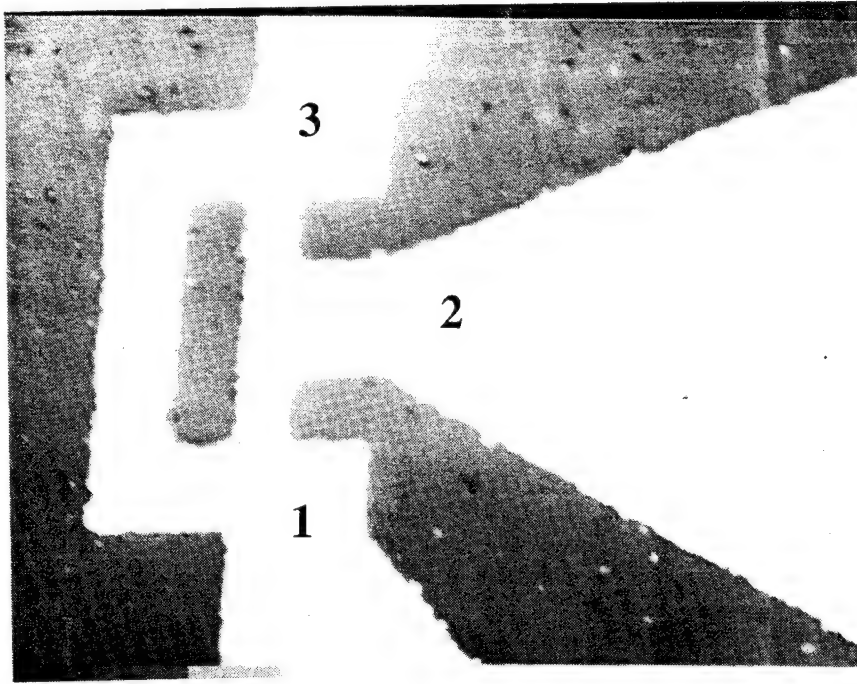


Fig. 18. SEM image of a SQUID fabricated on silicon from e-beam modified Josephson junctions.

DC Characterization

Fig. 19 shows the R vs T of this device, measured before and after e-beam modification. The graph shows that the e-beam process reduced the T_c of this device from approximately 80 K to 46 K. Other SQUIDs fabricated on lanthanum aluminate have maintained critical temperatures to over 80 K. The results are apparently extremely sensitive to the initial film quality. In light of this, steps would be taken in Phase II to improve the quality and uniformity of the films used for the junction experiments. (These remarks hold equally for the step-edge SNS junction work as well.) Fig. 20 shows the IV curves for two e-beam junctions with different critical temperatures from two different silicon chips.

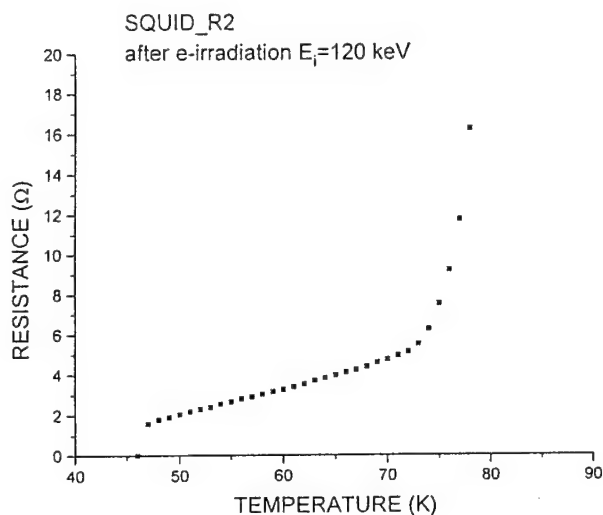
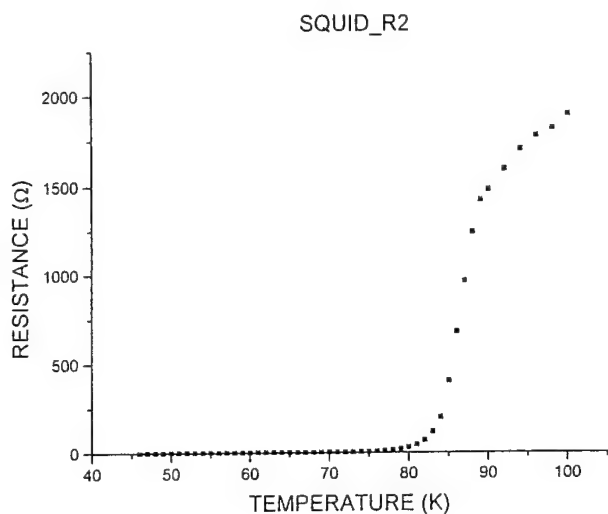


Fig. 19 R vs T curves of an e-beam modified SQUID fabricated on a silicon substrate measured before and after e-beam patterning.

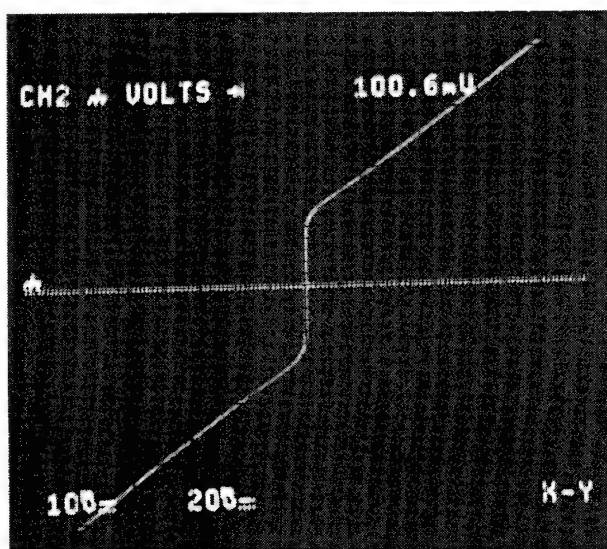
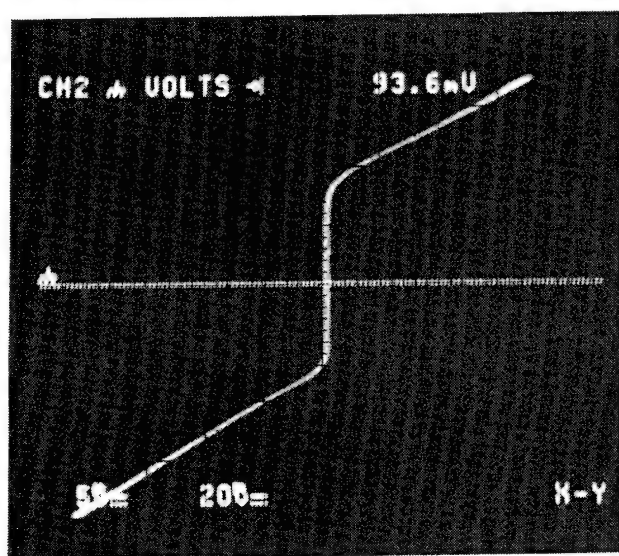


Fig. 20 (a) shows an I-V curve for a SQUID with a T_c of 46 K, measured at 39 K. The figure shows a finite critical current of 40 μ A, and a resistance of 0.8 Ω . 20 (b) shows results for another SQUID with a critical temperature of ~ 65 K, measured at 61 K. This SQUID had a critical current of 22 μ A and a resistance of 1.4 Ω .

RF Characterization

Fig. 21 shows the I-V curve for the SQUID of Fig. 20 (b) at 54 K, under microwave irradiation. Noise rounded Shapiro steps are clearly visible, confirming the existence of Josephson coupling across the SQUID.

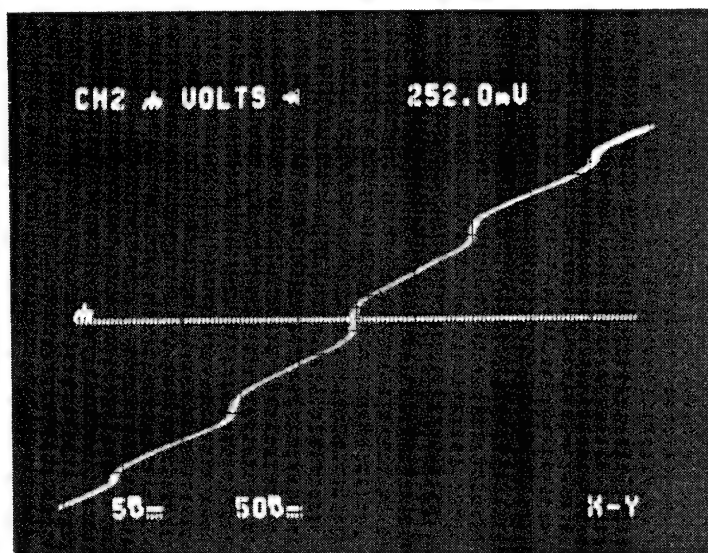


Fig. 21 Microwave induced steps in the IV curve of an e-beam junction on silicon.

Magnetic Field Modulation

Another test of the Josephson effect is to measure the response of a junction to an applied magnetic field. The detailed shape of the I_c vs H curve can be related to the uniformity of the critical current density as a function of position in the junction. Fig. 22 shows the measured I_c vs H for a single junction that was cooled below T_c in the ambient terrestrial magnetic field of ~ 0.5 G. For comparison, we show in fig. 23 the behavior expected for a hypothetically uniform 10 micron wide junction in a perpendicular field, taking flux focusing into account [26]. The measured result is in reasonable agreement with the theoretically expected behavior, given the fact that the electrodes were undoubtedly riddled with trapped fluxoids, and that there was certainly some degree of nonuniformity in the critical current density.

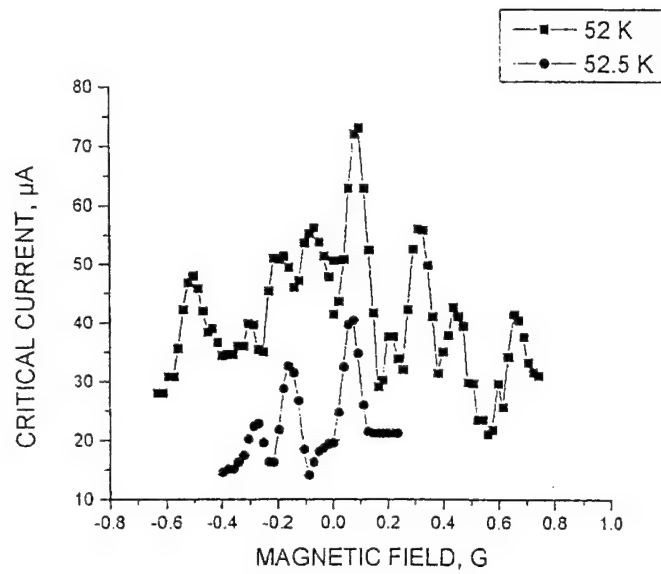


Fig. 22. Magnetic field modulation of the critical current of an e-beam modified junction fabricated on a silicon chip.

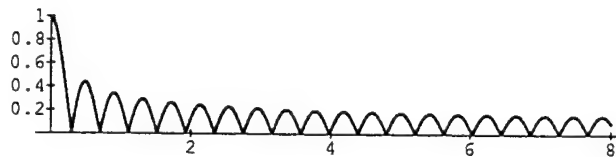


Fig. 23. Theoretical magnetic field modulation of an RSJ modeled junction in a perpendicular field when the film thickness is much thinner than the width and the penetration depth. From ref [26]

Cleaner results are apparent in measurements of SQUID R2, shown in Fig. 24. This SQUID was measured at 32 K, and the magnetic modulation was achieved through direct current injection through leads 1 and 3 (see Fig. 18). This measurement clearly shows the sinusoidal voltage modulation expected of a two junction interferometer. The flux in the SQUID loop is equal to the product of the loop inductance and the loop current. Since we are injecting the loop current directly, this gives us a direct method to measure of the SQUID loop inductance. In one period of the oscillation, the flux in the loop changes by one flux quantum $\Phi_0 = h/2e \approx 2.07 \text{ pH} \cdot \text{mA}$. Thus for the $50 \text{ } \mu\text{A}$ modulation period, we infer that the SQUID loop inductance was 41 pH . This is approximately a factor of two higher than that seen with SQUIDs fabricated on conventional substrates i.e. LaAlO_3 , however, given the uncertainties in the film thickness, these results are in reasonable agreement. From similar measurements performed as a function of temperature, we can distinguish the contribution due to kinetic inductance from the nearly temperature independent geometric inductance (there is a small temperature dependence to the geometric inductance due to the magnetic field energy stored within the temperature dependent penetration volume of the superconducting films.) Fig. 25 shows the temperature dependence of the SQUID inductance for two SQUIDs. SQUID_1 was an interferometer fabricated on a silicon substrate, RSFQ-1 was fabricated on a LaAlO_3 substrate by the barium fluoride/post-annealing technique. The difference in magnitude of these two results is mostly due to the different loop sizes, and hence the different geometric inductances. The divergence of inductance approaching T_c from below is a signature of the diverging kinetic inductance caused by the divergence of the penetration depth. The curved line in the figure is a fit to the two fluid model [23] in which the penetration depth is assumed to follow the relation: $\lambda_L(T) = \lambda_L(0) \left[1 - (T/T_c)^4 \right]^{-1/2}$. This analysis shows that the two fluid model provides a reasonable description of the temperature dependence of the loop inductance. This information will be useful in developing equivalent circuit models.

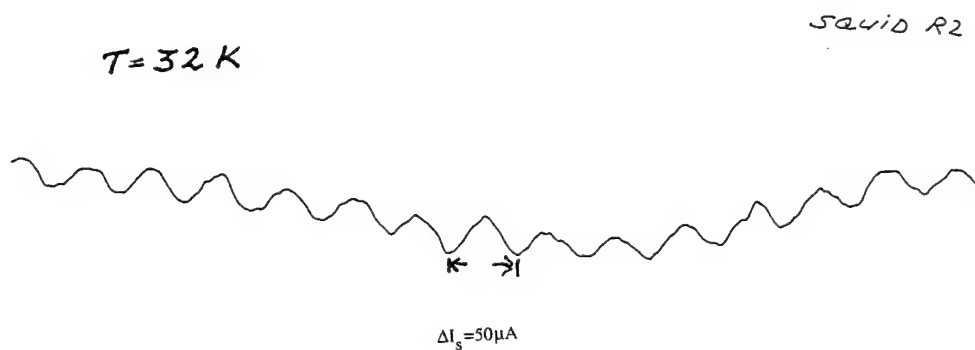


Fig. 24. Two junction interference pattern measured from an e-beam SQUID on silicon substrate. The modulation was achieved by direct current injection across the SQUID loop.

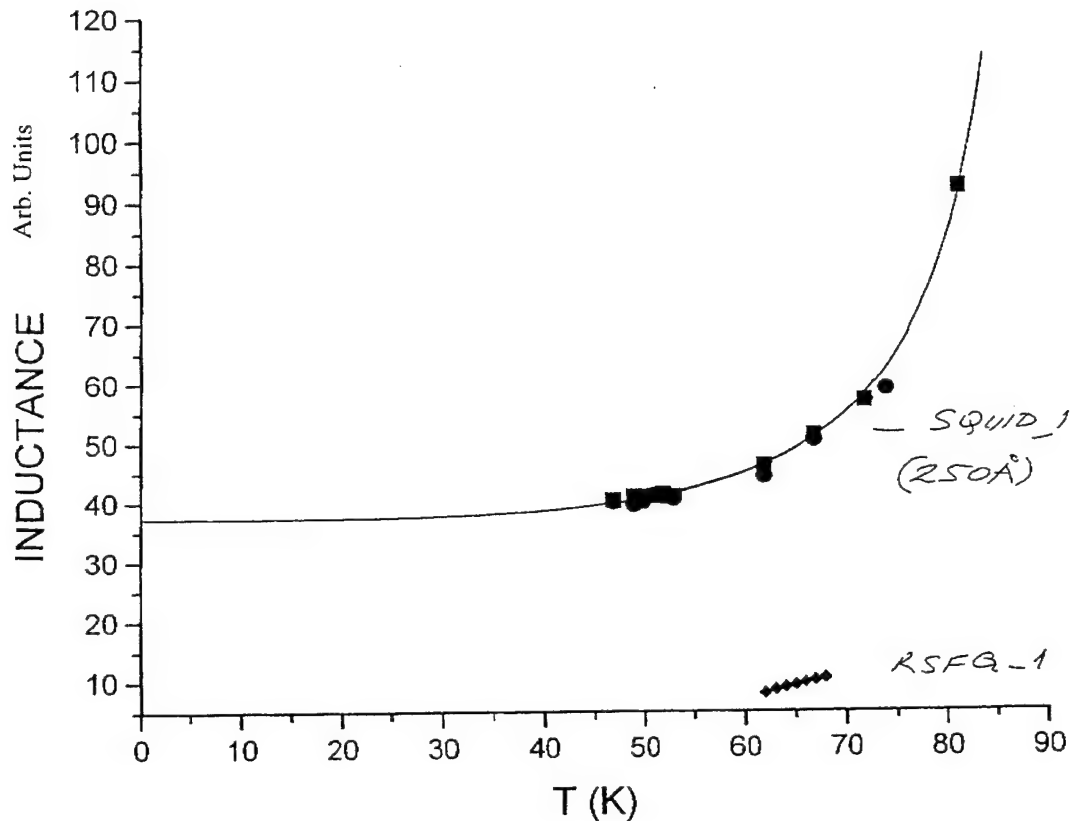


Fig. 25. SQUID inductance measured as a function of temperature and fit to the two fluid model.

3.c. Task 3 - Junction Modeling

Objective

To develop appropriate equivalent circuit models for HTS junctions on silicon substrates and to verify that the resistively shunted junction model adequately describes the dc and microwave properties of the junctions.

Results

In this section we will show quantitative agreement between the measured rf behavior of the step-edge SNS junctions on silicon and the predictions of the resistively shunted junction model. This will allow us to construct an equivalent circuit model suitable for use in rf and far infrared design applications.

In the RSJ model, the junction is modeled with the lumped equivalent circuit pictured in Fig. 26. There are four parallel elements: 1) a shunt capacitance, 2) a shunt resistance, 3) a Josephson current source, and 4) a noise source associated with thermal and other random processes within the junction [23].

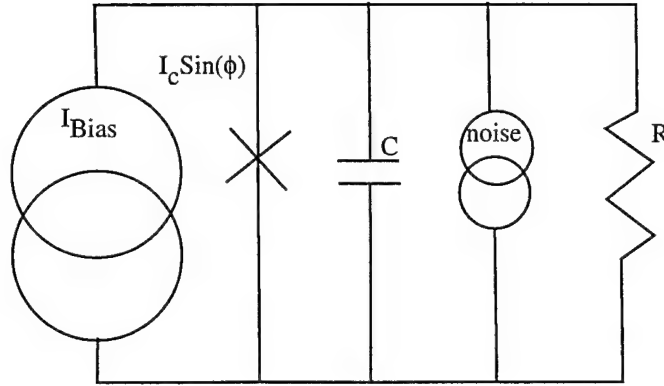


Fig. 26 Schematic of the RSJ model.

1) Capacitance - For the junction geometry under study, where the superconducting electrodes do not overlap, the junction capacitance is negligible.

2) Shunt resistance - In previous work, the PI and coworkers showed that there are two contributions to the conductance across a step edge junction, an intrinsic conductance associated with the supercurrent paths, and an additional parasitic parallel conductance associated with the currents that couple across the gold through the top surfaces of the YBCO electrodes[27]. An expression was derived for the parasitic shunt conductance across a step edge SNS junction that included the effects of boundary resistance across the superconductor/normal interface and series resistance within the normal conductor:

$$R_{\text{parasitic}} = \frac{2}{w} \sqrt{\frac{R_B \rho_n}{t}} \quad (1)$$

In the above expression, w is the junction width, R_B is the specific contact resistance between the gold and the YBCO, ρ_n is the resistivity of the gold, and t is the thickness of the gold. Removal of this parasitic conductance is achieved by removal of the gold overlapping the top surfaces of the YBCO. In reference [27], dramatic improvements in the junction properties were attained in this manner, increasing the characteristic voltage $I_c R_N$ by a factor of 10. Given that our best junction had an $I_c R_N$ product of $84 \mu\text{A} * 0.6 \Omega = 50 \mu\text{V}$ before this procedure, we expect to be able to fabricate junctions with characteristic voltages of at least 0.5 mV and probably higher.

The Josephson current source - The Josephson currents are determined by the dc and ac Josephson relations:

$$I = I_c \sin(\phi) \quad (2)$$

$$\dot{\phi} = \frac{2e}{h} V$$

Where ϕ is the Josephson phase, V is the instantaneous voltage across the junction, I_c is the junction critical current, and e and h are the electronic charge and Plancks constant, respectively.

Noise currents - There are many potential noise sources in a Josephson junction. External sources can couple large amounts of noise into a junction thanks to large bandwidths associated with the Josephson dynamics. The resistors themselves can contribute thermal noise, trapped flux in the films can fluctuate, injecting time varying currents into the junctions. In addition to these noise sources, defects within the junction can cause the critical current to fluctuate in time (this effect would be incorporated into the Josephson current source).

Microwave Induced Shapiro Steps

The measurements of the Shapiro steps provide a sensitive test of the ideality of the Josephson relations. If equations (2) do not hold rigorously, i.e. if the Josephson current-phase relation is not perfectly sinusoidal, then the power and frequency dependence of the microwave induced Shapiro steps would be expected to deviate from the predictions of the RSJ model.

To verify the applicability of the RSJ model for our SNS junctions, we measured the microwave rf power dependence of the critical current and the first Shapiro step. The results are shown in Fig. 27. The figure shows that as the microwave power was increased from zero, the critical current dropped continuously to zero, and rose and dropped back to zero with a Bessel function like behavior. Simultaneously, the first step went through more than one complete lobe as well. This behavior is generally expected from a resistively shunted junction, and is typical of what is observed for junctions grown on oxide substrates. For comparison, consider Fig. 28 (from reference [28]) which shows RSJ calculations of the rf current dependence of the critical current for several normalized rf frequencies $\Omega = \frac{hF}{2eI_C R_N}$. The normalized

frequency for our data in Fig. 27 is 0.44, as calculated from the dc junction properties and the known microwave frequency. Note the similarity between our data and the curve labeled $\Omega=0.4$ in Fig. 28. This demonstrates that our junction measurements are in good agreement with the RSJ model. Another quantitative test that can be made is in the spacing of the zeros of the critical current and Shapiro steps[29]. Fig. 29 shows the results of an RSJ calculation of the parameter $\kappa_n = I_{n,2}/I_{n,1} - 1$ as a function of reduced frequency for the critical current ($n=0$) and the first two Shapiro steps ($n=1,2$). κ_0 is computed from the ratio of the first two zeros of the critical current (i.e. $I_{0,2}$ and $I_{0,1}$ are the rf currents associated with the first and second zeros of the critical current). Our data is shown as a point on this plot. The quantitative agreement between the measured junction behavior and the RSJ model is excellent.

The modeling work performed in Phase I shows that the RSJ model can be used for design and analysis of circuits using our step-edge SNS junctions. Because of this, analysis and simulations of more complicated structures involving junctions, resonators, filters and other passive structures as well as external rf sources can be performed with confidence using the RSJ model.

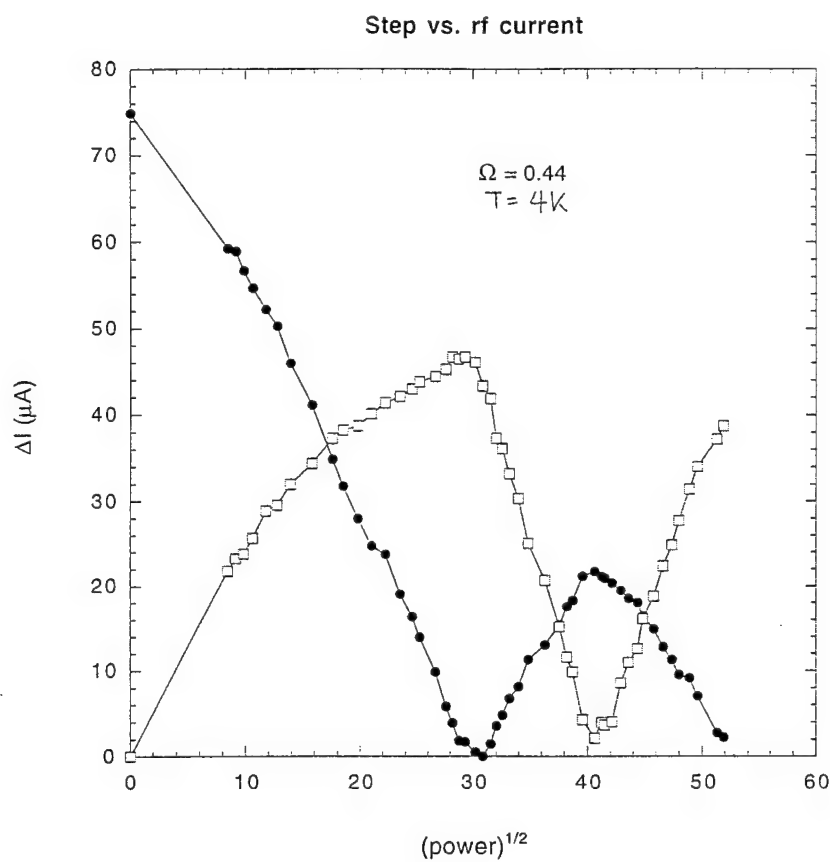


Fig. 27. Measured rf current dependence of the microwave induced steps in the current voltage characteristics at 4 K and 8.3 GHz for a step-edge SNS junction on silicon.

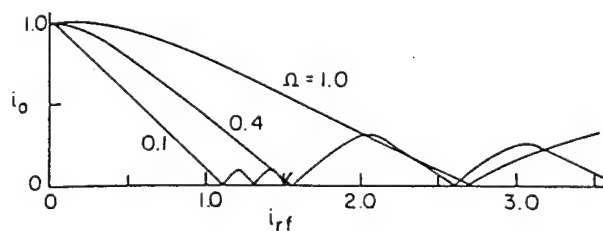


Fig. 28. RSJ modeled rf current dependence of the microwave induced steps for different normalized frequencies.

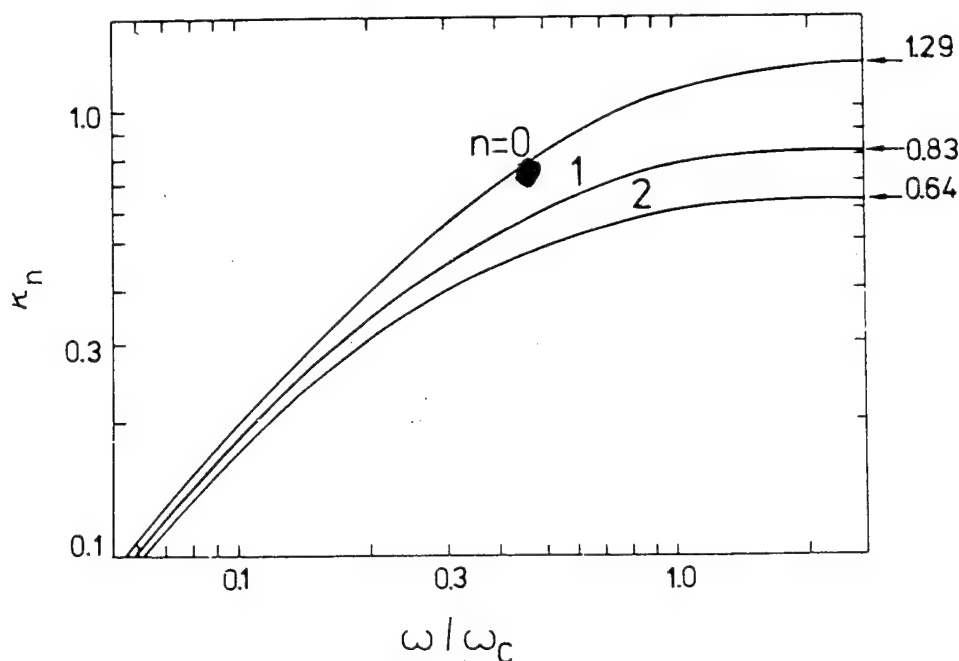


Fig. 29. RSJ analysis of the frequency dependence of the zeros of the critical current and Shapiro steps. The solid point was computed from the measurements in Fig. 27. From Ref [29].

3.d. Task 4 - Design Study

Objective

To demonstrate the feasibility of integrating HTS active and passive components on a silicon wafer

Results

For the Phase I design analysis, our focus was on identifying the technology areas that would benefit the most from combining the large area, relatively low dielectric constant and low cost of silicon substrates with the unique properties of HTS active and passive components. The use of silicon is expected to be especially advantageous for system level components combining multiple passive microwave components with active components. For these applications, the real estate requirements of the passive filters, delay lines, antennas etc. can be substantial and can easily outstrip the available sizes of more exotic substrate materials such as LaAlO_3 . Many of these circuits, e.g. downconverters and mixer subsystems could be implemented monolithically, using Josephson junctions as the active components. Other applications requiring amplification might also require semiconducting active components. One of the goals of the Phase II effort will be to identify which semiconducting devices are monolithically compatible with HTS processing and which (including III-V's) will require hybrid bonding.

We identified two areas where significant and relatively rapid innovations could be made possible from this research: 1) integrated microwave downconverters and receiver front ends, and 2) *Monolithic* quasi-optimally coupled microwave and millimeter wave imaging and non-imaging spectrometers.

Integrated Microwave components

A Josephson Downconverter

An rf downconverter is a device that takes a microwave signal with an encoded digital or analog stream, mixes it with a local oscillator using a nonlinear element, and outputs a decoded analog or digital stream. Downconverters play a central role in wideband telecommunications systems. The components in a downconverter are a local oscillator (LO); a filter network comprising the LO feed, the rf signal feed, and the output port; and a dc bias network.

An experimental system developed by AT&T utilized HTS or Au thin film filter banks, a flip chip bonded GaAs Schottky diode as a nonlinear mixer, packaged in a custom waveguide mixer block [30]. These devices had impressive performance, demonstrating low-error data transmission rates of 1.8 Gbits/sec with a 20 GHz carrier frequency. Several difficulties associated with the substrates were encountered in this work. Bonding GaAs devices to the lanthanum aluminate substrates was difficult, and the substrates were fragile, expensive, and cracked frequently on cooldown. The contacts were unreliable when subjected to repeated thermal cycling. The improved filter performance enabled by HTS thin films helped justify the extra manufacturing complexity required for superconductor integration. Replacing the GaAs Schottky diode mixer with an integrated HTS Josephson mixer would resolve some of the reliability issues and the problems associated with the lanthanum aluminate substrate itself (breakage, crystallographic twinning, high dielectric constant ($\epsilon_r = 25$), etc.) would be greatly alleviated by the utilization of silicon substrates.

A Dual Channel Receiver Front End

A more complicated wafer scale system developed by Dupont[31, 32] illustrates further some of the potential advantages of adopting silicon substrates for HTS rf electronics. Fig. 30 shows a dual channel X-band hybrid receiver front end fabricated from a double-side YBCO coated three inch lanthanum aluminate wafer. This hybrid subsystem incorporated HEMTs, schottky diodes, and many passive components. Clearly, the availability of large, inexpensive wafers with good mechanical and rf properties compared to lanthanum aluminate would greatly impact the manufacturability and performance of these large wafer scale subsystems.

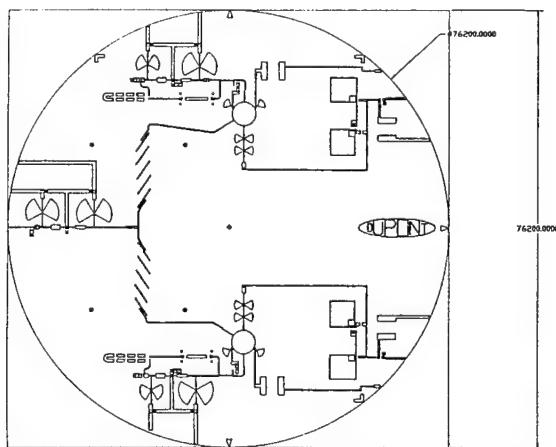


Fig. 30. An X band dual-channel receiver front end fabricated from a double-side YBCO coated 3 inch lanthanum aluminate wafer. From Ref [2].

New Josephson RF Applications

Although replacing GaAs mixers with a monolithically integrated Josephson mixers would in itself improve reliability and manufacturability, there are other reasons to replace semiconducting active devices with HTS based Josephson active devices. These are cases where one can exploit the unique properties of superconducting devices in structures that have no semiconductor. For example, Josephson mixers can be operated in a unique self-pumped mode where the ac Josephson oscillations serve as the local oscillator, and the intrinsic nonlinearity of the Josephson effect provides the mixing action. This mode of operation eliminates the local oscillator and accompanying coupling structures required in more conventional heterodyne receiver architectures, and could potentially result in great system simplifications. Self pumped mixers could be implemented with either single junctions or with phase locked arrays to achieve narrower linewidths and higher channel density.

Quasioptically Coupled Josephson Electronics

Josephson junctions have many potential applications as detectors for signals ranging from microwaves through infrared waves. For these applications, it is often useful to integrate planar antennas on the substrate with the junctions themselves. Such structures can be used in either bolometric or non bolometric configurations, depending on the frequency ranges of interest.

In one novel non-bolometric application, an innovative quasioptical millimeter/submillimeter "spectrometer on a chip" could be fabricated and integrated into an imaging spectroscopic focal plane array. Such self pumped Josephson mixers can also be fashioned using coherent junction arrays, allowing greatly reduced linewidths and spectral resolution.

HTS Josephson Junction Hilbert Transform Spectrometer --

The Josephson Hilbert transform spectrometer is a novel spectrum analyzer based on the Josephson effects [33,29]. The simplest version of this device is a Josephson junction integrated at the feed of a frequency independent antenna. Fig. 31 (a) is a sketch of a single antenna coupled junction pixel element. Fig. 31 (b) is a sketch of a 256 element imaging array (coupled through the substrate backside) at the focal plane of a hemispherical lens. (c) shows a schematic view of the quasioptical coupling scheme. The junctions in Fig. 31, being too small to be seen, are not depicted, and the detector chip and lenses are not drawn to accurate scales.

The operation of the Hilbert transform spectrometer is based on the small signal nonlinear response of a Josephson junction to an rf signal. The response of a Josephson junction's dc iv curve to an rf signal in the presence of noise has been well studied in the RSJ model [29]. The overall junction response is due to interactions between four currents: the dc bias, the rf signal, noise sources, and the internal Josephson oscillations. For large rf currents, the junction dynamics are dominated by the phenomenon of phase locking, resulting in the appearance of the well known Shapiro steps in the iv curve. For small rf currents in the presence of noise, however, the phase locking is not perfect and only the "embryo" of a single Shapiro step, related to the rf frequency, forms in the IV curve. The dc response is quadratic in the rf current. When the noise is smaller than the rf currents, then the current responsivity to a monochromatic signal of angular frequency is given by [29, p322]:

$$\rho_I = \frac{\Delta I}{I_\omega^2} = \frac{V_c^2}{4I(V_1^2 - V^2)} \quad (3)$$

Here I is the observed change in the dc current due to the application of the rf current of magnitude I , I and V are the current and voltage of the autonomous (with no applied rf signal) iv curve, $V_c = I_c R_N$ is the junction characteristic voltage, and $V_J = h/2e$ is the dc Josephson voltage corresponding to the applied frequency.

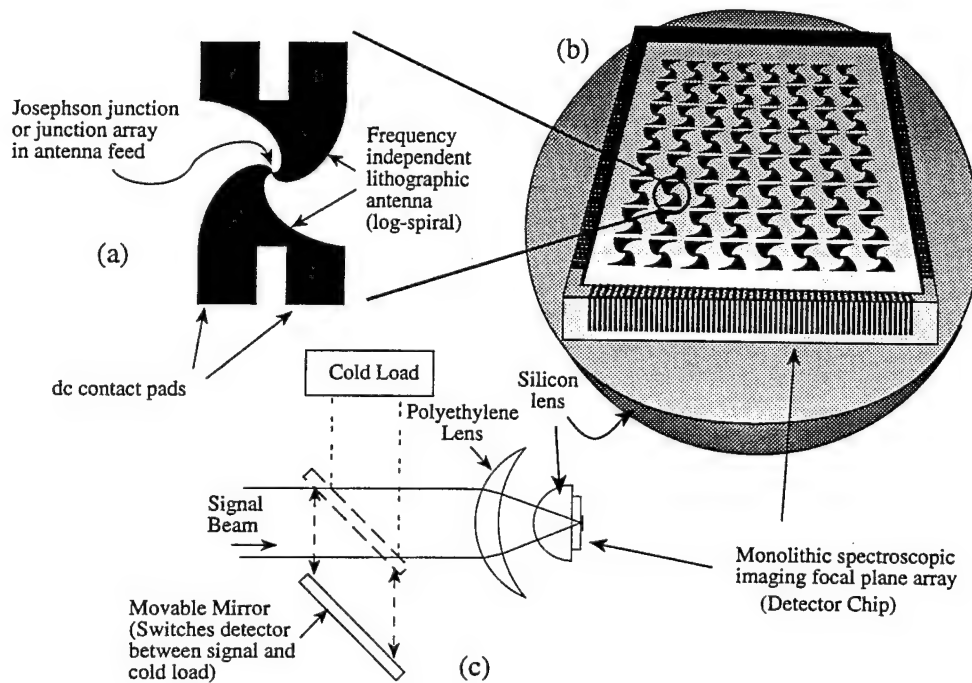


Fig. 31 (a) Sketch of single pixel element of a Josephson Hilbert transform spectrometer with a frequency independent log-spiral antenna. (b) Sketch of a 256 element spectroscopic imaging focal plane array. (c) Sketch of the quasi optical coupling scheme for a Hilbert transform spectrometer.

Using Eq. (3), one can show that a quadratic superposition principle holds for spread spectrum rf currents. Specifically, if we define the spectral density of the rf signal as:

$$I(t) = \text{Im} \sum_{\omega} I_{\omega} e^{j\omega t} \quad (4)$$

$$\text{and defining } \Delta I = \sum_{\omega} \rho_I(\omega) |I_{\omega}|^2 \quad (5)$$

Then one can show that the current response and the frequency spectrum of the applied signal are related by a Hilbert Transform:

$$\Delta I * I(V) * V \propto \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{S_I(\omega)}{\omega - \frac{2e}{\hbar} V} d\omega \quad (6)$$

and because the Hilbert transform is its own inverse, we can solve for the signal spectral density in terms of the measured junction response function:

$$S_I(\omega) \propto \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{\Delta I * I(V) * V}{\omega - \frac{2e}{\hbar} V} dV \quad (7)$$

The remarkable result is that the spectral density of a spread spectrum rf signal can be determined by a simple integral transform of a response curve easily extracted from the junction iv curve. Fig. 32 shows results reported by Divin et al [33], of a waveguide coupled low temperature superconducting Hilbert transform spectrometer irradiated with a mixture of three monochromatic signals. The top trace shows the junction iv curve with and without the signal, the middle shows the computed response function, and the bottom trace shows the extracted signal spectral density (the Hilbert transform of the middle trace), correctly reproducing the spectrum of the applied signal. This work demonstrates the feasibility of the concept. In Ref [33], Divin et al reported a frequency resolution of order 0.5 GHz, which is about what the RSJ model predicts, assuming that the Josephson linewidth is broadened primarily through the action of thermal fluctuations. This analysis can be extended to include the effects of noise. The main effect of noise currents is to limit the attainable frequency resolution to the noise induced linewidth of the Josephson oscillations. On the basis of general thermodynamic arguments, the minimum Josephson linewidth for a single junction at 77 K will be ~3 GHz per ohm of junction resistance [29]. This prediction has been experimentally confirmed. There is also an opportunity to achieve higher spectral resolution by incorporating arrays rather than single junctions. Through the use of quasioptical coupling and planar lithographic antenna arrays, it should be possible to adapt this technology to spectral imaging arrays for the microwave through far infrared frequency ranges.

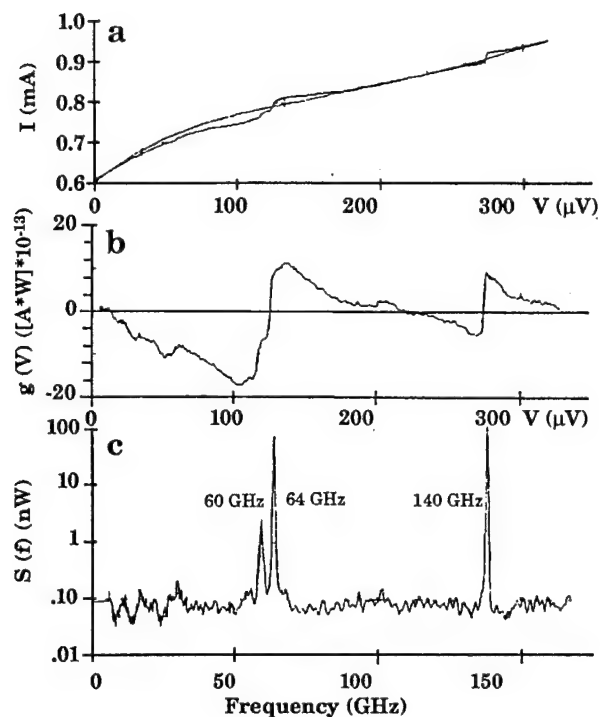


Fig. 32 Spectrum measurements of a mixture of three monochromatic signals (from [33]).

Design Issues--

We must couple rf currents into a Josephson junction across the entire spectral region of interest, while simultaneously performing precise measurements of the dc iv characteristics. The dc measurements will be straightforward providing we can employ the usual 4 contact method. The rf currents will be coupled quasioptically via an antenna. For imaging at mm and submm wavelengths, quasioptical coupling through the backside of the substrate to an integrated lithographic antenna is the method of choice [34]. Antenna coupling allows wide signal bandwidths, it can be integrated monolithically with the junction, and the extension to imaging and non-imaging focal plane arrays is straightforward. Planar lithographic antennas can be designed to have a frequency independent, purely real impedance over arbitrary bandwidths by making them self-similar and self-complementary, i.e. the open spaces have the same shape as the metalized regions. One of the simplest and best characterized wideband antennas for short wavelengths is the self-complementary log-spiral antenna, shown in Fig. 1(a). Excellent antenna efficiency on a silicon substrate has been demonstrated down to $10.6 \mu\text{m}$ wavelengths[35]. In Fig. 31(c) we depict the quasioptical coupling scheme, showing how the signal beam is coupled through polyethylene and silicon lenses, with an insertible cold load (to measure the iv curve with no rf current). In previous related studies, the PI has demonstrated that a properly designed planar log-periodic is capable of coupling signals ranging from 400 GHz to 992 GHz into HTS junctions [36]. We are confident that this method can be adapted to frequencies from the GHz range up to several THz. Fig. 33 shows a junction integrated at the feed of a log-periodic antenna, fabricated on a lanthanum aluminate substrate. This type of device demonstrated efficient power coupling from approximately 400 GHz to 1 THz when tested at NIST by the PI.



Fig. 33. Optical micrograph of a log-periodic antenna-coupled step-edge SNS Josephson junction fabricated on a lanthanum aluminate substrate [36].

4. TECHNICAL RECOMMENDATIONS AND ANTICIPATED PHASE II PROGRAM

The Phase I program clearly demonstrated that it is possible to fabricate high quality YBCO Josephson junctions on silicon substrates. The anticipated Phase II program would have several thrusts that build upon the achievements of Phase I. The tentative Phase II effort would be performed by a team composed of AFR, NIST, SUNY Stony Brook, and AT&T. We have discussed the program with Professor Gurvitch at Stony Brook; Dr Ron Ono, Dr. Dave Rudman and Dr. Jack Ekin at NIST; and with Dr. Paul Polakos at AT&T Bell Laboratories. They are all interested in participating in the Phase II program. The personnel, and organizational strengths are summarized in Table 2.

Organization	Personnel	Areas of expertise	Program function
AFR	Dr. Peter Rosenthal Dr. Dave Fenner	<ul style="list-style-type: none"> • Josephson junctions • HTS thin films on silicon • Superconducting Electronics • Infrared applications of HTS 	<ul style="list-style-type: none"> • Program management • Junction fabrication • Buffer layer technology • Device testing • Hilbert Transform Spectrometer design and fabrication
NIST	Dr. Ron Ono Dr. Dave Rudman	<ul style="list-style-type: none"> • Step edge Josephson Technology • Device Fabrication • Film Characterization • HTS microwave properties • HTS metrology 	<ul style="list-style-type: none"> • Circuit layout and fabrication • Device testing • Microwave measurements • rf testing of Hilbert transform spectrometer and Josephson mixers.
Stony Brook	Dr. M. Gurvitch Dr. K. Likharev Dr. S. Tolpygo	<ul style="list-style-type: none"> • E-beam junction fabrication • Josephson technology • Modeling of Josephson junctions and superconductors • HTS materials 	<ul style="list-style-type: none"> • E-beam junction fabrication • Junction modeling • Junction testing
AT&T	Dr. Paul Polakos Dr. Paul Mankiewich	<ul style="list-style-type: none"> • Microwave applications of superconductivity • Telecommunications 	<ul style="list-style-type: none"> • Downconverter design and testing • Transmission line characterization • System integration

Table 2. Organizational Chart of Tentative Phase II program

Following is a summary of the areas that we would address in the Phase II program.

1. Junction Optimization - Both types of junctions were fabricated in Phase I without full systematic optimization of the yield or electrical properties. In Phase II working with our colleagues at NIST and Stony Brook we would optimize the fabrication process. When the fabrication yield, reproducibility and electrical properties of the junctions are under better control, then we will be in an excellent position to exploit these devices in more complex circuits. As discussed in section 3, to optimize the junction

fabrication we will perform more systematic exploration of the step fabrication, surface treatment, film deposition, and e-beam process parameters.

The team for this work would be a three-way effort involving NIST, Stony Brook and AFR, essentially the same team that performed the Phase I research.

2. Film stress relief - As discussed in section 2, we believe that film stress from thermal expansion coefficient mismatch is a major hurdle for HTS films on silicon. We would like to describe our proposed solution to this problem, to be attacked in Phase II.

The heart of the problem is that silicon has a smaller thermal expansion coefficient than YBCO. This puts the YBCO film under severe tensile strain during cool-down from the growth temperature. The yield strength for YBCO decreases as the film gets thicker, so beyond some critical thickness, cracks will inevitably appear if the stress can only be relieved elastically. Our solution is to allow plastic flow between the silicon substrate and the YSZ buffered YBCO film. This will be achieved through the introduction of a novel plastically deformable buffer layer.

The buffer layer will consist of a thin film of a glass situated between the silicon substrate and the YSZ/YBCO bilayer. The soft glass film will be chosen to have a strain annealing temperature well below the growth temperature. The structure and its fabrication are depicted in Fig. 34. The fabrication of the buffer layer will involve the processes of film deposition and wafer bonding.

First, a silicon wafer is coated with a YSZ film. This wafer is then bonded as shown to another silicon wafer that was previously coated with a thermal oxide or some other glass layer. Next, the first wafer is then etched back to the YSZ film. This can be accomplished with a wet KOH etchant, which will quickly dispose of the silicon wafer but will not etch through the YSZ at all. After cleaning and possibly spin-etching the YSZ surface, we should be able to deposit YBCO on the YSZ film, which will now be floating on a deformable glass layer, rather than being directly coupled to the silicon substrate.

In this structure, the HTS and YSZ layers can contract faster than the substrate during cooldown, and the glass film will accommodate the strain by deforming plastically.

If successful, this strain relief technology will be a significant breakthrough for rf applications of HTS thin films with revolutionary implications for the nascent HTS microelectronic industry. Further applications are expected to be found in other strained thin film materials including ferroelectrics, III-V nitrides, diamond, and other exotic semiconductors.

NIST has agreed to collaborate on this facet of the research, and we have discussed the implications of this concept with Dr. Paul Polakos of AT&T Bell Laboratories. He is interested in performing measurements of coplanar wave guide and microstrip transmission lines fabricated from HTS thin films on silicon, and is particularly excited by the prospect of thick, low surface resistance materials on silicon.

In the Phase II program, we would fabricate these compliant substrates and investigate their use for HTS thin films.

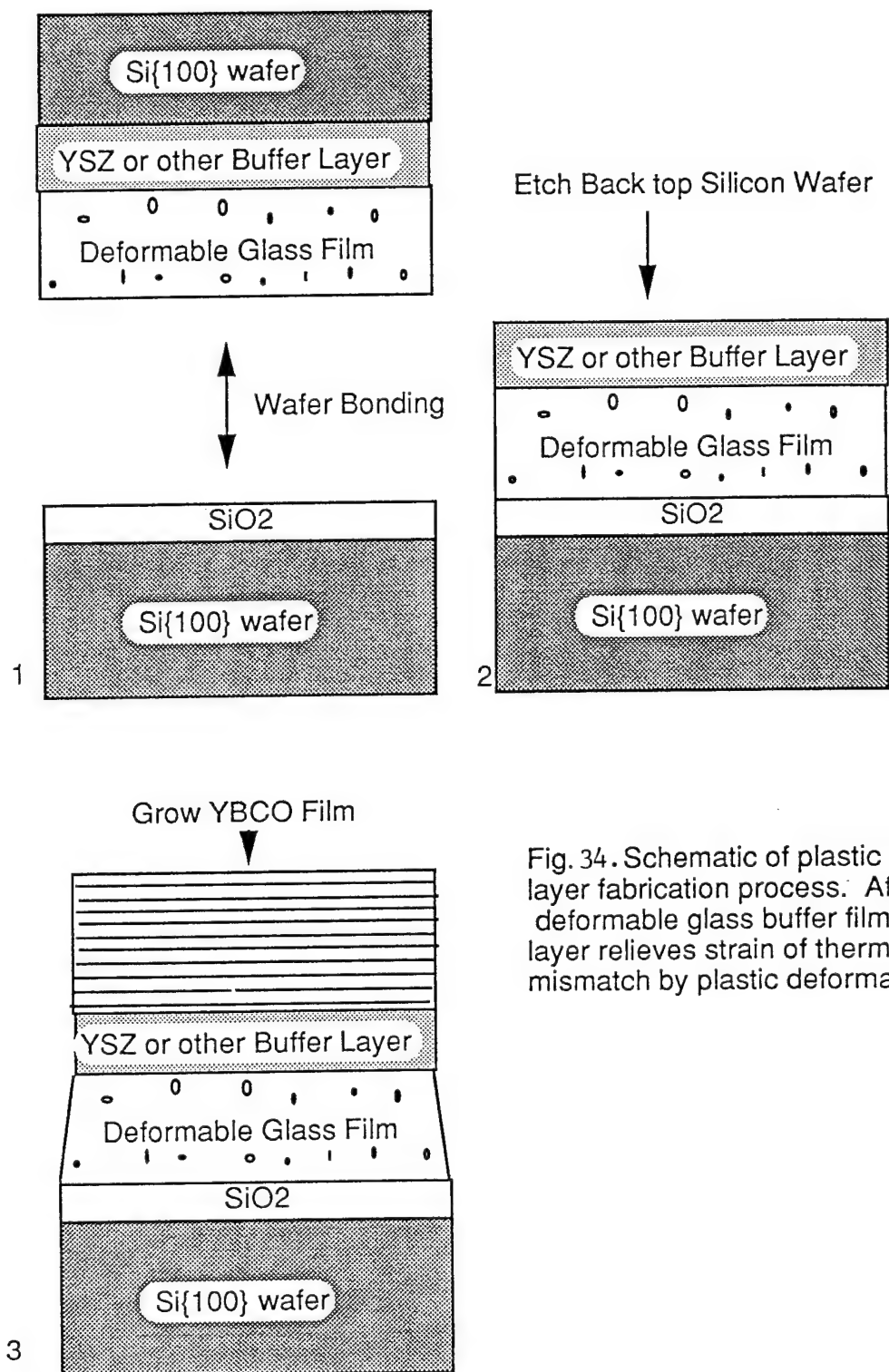


Fig. 34. Schematic of plastic buffer layer fabrication process. After growth, deformable glass buffer film layer relieves strain of thermal expansion mismatch by plastic deformation.

3. RF devices -

Passive Components - Working with AT&T, we would design and fabricate circuits combining Josephson devices with HTS passive components. This work would involve first fabricating and characterizing resonators, filters and other passive components by themselves. As the thicker films on silicon become available, these activities are expected to become extremely important, with strong commercial possibilities.

Integrated Systems - Working with AT&T and NIST, we would design, fabricate and test a microwave upconverter and downconverter for rapid digital data modulation and demodulation. The circuit would be based on HTS Josephson active components, and either gold or YBCO filters and passive components, depending on the design simulations.

Mixer Technology and novel applications of the Josephson effects - Working with NIST, we would design, fabricate and test Josephson mixers for the microwave through far infrared frequencies. We would explore self-pumped mixers and fabricate a Hilbert transform spectrometer.

Detectors - We would build and test an antenna coupled Josephson bolometric infrared detector for use in Fourier transform infrared (FT-IR) and imaging applications.

Digital Applications - Stony Brook would pursue high speed RF and RSFQ digital circuits based on e-beam junctions on silicon.

5. FORTHCOMING PUBLICATIONS AND PRESENTATIONS OF THE RESULTS

MRS -- 1995 FALL MEETING -- NOV 27-DEC 1 -- BOSTON

SUBMITTED TO SYMPOSIUM G

SYMPOSIUM TITLE: EPITAXIAL OXIDE THIN FILMS II

HIGH TEMPERATURE SUPERCONDUCTING STEP-EDGE SNS JOSEPHSON JUNCTIONS ON SILICON SUBSTRATES, P.A. Rosenthal, J.E. Cosgrove, and D.B. Fenner, Advanced Fuel Research, Inc, East Hartford, CT; and L.R. Vale, R.H. Ono and D.A. Rudman, NIST, Boulder, CO.

We have fabricated and tested YBCO step-edge SNS Josephson junctions on silicon substrates. The silicon step edges were patterned photolithographically and reactively ion etched using an SF₆ plasma. The structures were fabricated through sequential angled pulsed laser deposition of yttria stabilized zirconia, YBCO, and gold layers, followed by photolithographic patterning and ion milling. The completed devices showed resistively shunted junction (RSJ)-like current voltage characteristics and microwave induced Shapiro steps. Critical currents as large as 84 μ A and resistances of order 0.5 Ω were obtained. Measurable critical currents were observed up to 76 K. We will report on the fabrication and properties of these junctions.

Oral Session Preferred

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1995 FALL MRS ABSTRACT

SUBMITTED TO SYMPOSIUM F

SYMPOSIUM TITLE: DEFECTS IN HIGH-TEMPERATURE
SUPERCONDUCTORS-
CHARACTERIZATION AND RELATIONS TO PROCESSING AND
PROPERTIES

YBCO FILM GROWTH ON SI SUBSTRATES FOR JOSEPHSON
JUNCTION FABRICATION, L.R. Vale, R.H. Ono, and D.A. Rudman,
National Institute of Standards and Technology, Boulder CO 80303 and
P.A. Rosenthal, J. E. Cosgrove, and D.B. Fenner, Advanced Fuel Research,
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We have studied the growth of $\text{YBa}_2\text{Cu}_3\text{O}_7$ (YBCO) on reactive ion etched Si substrates. We use Pulsed Laser Deposition (PLD) to deposit YBCO on yttria-stabilized zirconia (YSZ) buffered (100) Si substrates. Previous YBCO growth studies on etched Si resulted in highly defective YBCO that was non-superconductive. Current YBCO growth conditions produce superconducting films with transition temperatures $T_c = 86\text{K}$ and critical current densities $J_c > 7 \times 10^5 \text{ A/cm}^2$ at 76K on the unetched Si surface. Although the T_c was similar on the etched Si surface, the J_c was greatly reduced ($\sim 5000 \text{ A/cm}^2$ at 4K). The films show numerous outgrowths and imperfections, evident in the YSZ layer also, which are caused by damage to the Si substrate incurred during the reactive ion etching process. Using these films, we have fabricated high- T_c superconductor-normal metal-superconductor (SNS) step edge Josephson junctions on Si substrates. The step edge is produced in the Si by reactive ion etching with SF_6/O_2 . We then deposit by PLD a 50 nm thick buffer layer of YSZ, followed by a 70 nm thick layer of YBCO and a 100 nm Au layer. The resulting SNS Josephson junctions had RSJ-like characteristics but the junction analysis was complicated by the occurrence of grain boundary junctions in series with the Josephson junctions. We are continuing work to improve the growth of YBCO on etched Si for junction fabrication.

Poster Session Preferred

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